DIGITAL VLSI IC DESIGN
(VLSI 5101)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) According to Moore's Law, number of transistor per chip gets doubled in
(a) 6 months (b) 12 months
(c) 18 months (d) 24 months.

(ii) Ideal current source has resistance of value
(a) 0 Ohm (b) Infinite
(c) 100 Ohm (d) 100 k-Ohm.

(iii) Most popular interconnect material is
(a) Gold (b) Silver
(c) Copper (d) Platinum.

(iv) For a standard cell layout
(a) width is fixed (b) height is fixed
(c) width and height are fixed (d) width and height are variable.

(v) Memory design is normally done using below method
(a) FPGA (b) Gate Array
(c) Full Custom (d) Std Cell Based Semi Custom.

(vi) Value of "Lambda" in 180nm Process Node is
(a) 180 nm (b) 90 nm
(c) 45 nm (d) 360 nm.

(vii) BDD is used in
(a) High Level Synthesis (b) Floorplaning
(c) Logic Synthesis (d) Partitioning.

(viii) Minimum number of transistors required to implement CMOS logic Y = ABE + CD is
(a) 10 (b) 12 (c) 14 (d) 16.

(ix) KL algorithm is related to
(a) High Level Synthesis (b) Floorplaning
(c) Logic Synthesis (d) Partitioning.

(x) Most manual effort is needed in below VLSI methodology
(a) full custom (b) standard cell based semi custom
(c) CPLD (d) FPGA.

Fill in the blanks with the correct word

(xi) Full form of PLA is _____.

(xii) MOS in saturation can be modelled as circuit element like _____.

(xiii) LUT stands for _____.

(xiv) Technical name of 3D transistor is _____.

(xv) In Domino Logic, Output of Dynamic Gate is connected with input of _____.

Group - B

2. (a) Implement circuit of a Level-1 D-Latch using CMOS Transmission Gate (TG). *[(CO1)(Evaluate/HOCQ)]*
(b) Implement circuit of a positive edge triggered D-Flip Flop using Level-1 D-Latch and any other digital gates. *[(CO1)(Evaluate/HOCQ)]*
(c) Implement circuit diagram of a 2 input XNOR gate using CMOS Transmission Gate (TG). *[(CO1)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

3. (a) Describe Y Chart. *[(CO3)(Remember/LOCQ)]*
(b) Implement schematic of CMOS gate which represents function f = (AB+C)´. *[(CO2)(Apply/IOCQ)]*
(c) Evaluate Stick Diagram of the same CMOS gate. *[(CO2)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

Group - C

4. (a) Draw flow diagram of VLSI design cycle. *[(CO3)(Remember/LOCQ)]*
(b) Draw flow diagram of front end design flow. *[(CO5)(Understand/LOCQ)]*
(c) Write VHDL behavioural model for a rising edge triggered D–flip flop. *[(CO4)(Apply/IOCQ)]*

4 + 4 + 4 = 12

5. (a) What are differences between full custom design and std cell based semi custom design. *[(CO3)(Remember/LOCQ)]*
(b) Evaluate Euler Path solution of a CMOS gate which represents function f = (AB+C+D)´. *[(CO2)(Evaluate/HOCQ)]*
(c) Implement stick diagram of the same CMOS gate based on euler path solution. *[(CO2)(Apply/IOCQ)]*

4 + 4 + 4 = 12

Group - D

6. (a) Draw flow diagram of High Level Synthesis. *[(CO5) (Remember/LOCQ)]*
   (b) Implement BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using Ordering of a $\leq$ b$\leq$ c. *[(CO5) (Evaluate/HOCQ)]*
   (c) Create ROBDD Diagram and corresponding optimized Boolean expression. *[(CO5) (Evaluate/HOCQ)]*

4 + 4 + 4 = 12

7. (a) Write VHDL code of behavioural modelling of a 2:1 Multiplexer. *[(CO4)(Apply/IOCQ)]*
   (b) Write VHDL code of behavioural modelling of a 2 input NAND Gate. *[(CO4)(Apply/IOCQ)]*
   (c) Explain technology library mapping for logic synthesis. *[(CO5)(Analyze/IOCQ)]*

4 + 4 + 4 = 12

Group - E

8. (a) Draw flow diagram of physical layout automation. *[(CO6)(Remember/LOCQ)]*
   (b) For below channel routing problem, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG)
   Terminal Connections are as follows:
   11122563040 ----- Upper Boundary
   25055330604 ----- Lower Boundary
   0 means no Connection.
   Assume HV Layer (V = Metal 1, H = Metal 2). *[(CO6)(Apply/IOCQ)]*
   (c) Provide Optimum Channel Routing Solution for above case using the Left Edge Algorithm. *[(CO6)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

9. (a) Explain the left edge algorithm for detailed routing. *[(CO6)(Understand/LOCQ)]*
   (b) Implement the 2 input XNOR operation using LUT of FPGA. *[(CO3)(Evaluate/HOCQ)]*
   (c) Explain I-V characteristics of MOS transistor. *[(CO1)(Analyse/IOCQ)]*

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	29.17	33.33	37.5

Course Outcome (CO):

After the completion of the course students will be able to
CO1. Students will learn CMOS Circuit used in Digital VLSI Domain
CO2. Students will learn Physical Layout Design of CMOS Standard Cell
CO3. Students will learn Digital VLSI Design Methodology
CO4. Students will learn HDL coding
CO5. Students will learn EDA High Level and Logic Level Synthesis Algorithms
CO6. Students will learn EDA Physical Place and Route Automation Algorithms.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*