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(viii)	A ring counter consisting of five Flip-Flops will have		
	(a) 5 states	(b) 10 states	
	(c) 32 states	(d) infinite states.	

- Shift registers having four bits will enable shift control signal for (ix) (a) 2 clock pulses (b) 3 clock pulses (c) 4 clock pulses (d) 5 clock pulses.
- (x) Maximum no of inputs connected to gate is called (a) fan (b) fan in (c) fan out (d) outcome.

Group - B

- Subtract the following using binary signed magnitude representation: 2. (a) $(23)_{10} - (38)_{10}$.
 - (b) Convert the following: (i) $(123.556)_8 = (?)_{16}$ (ii) $(A2BF.CC5)_{16} = (?)_8$
 - (i) Find the IEEE 754 Floating point (32 bits) representation of (c) $(13.625)_{10}$.
 - (ii) Find out the Decimal Number for which the IEE 754 Floating point representation is as follows:

S	Е	М
0	10000010	101101

4 + 3 + 5 = 12

- 3. (a) Convert the decimal number 45678 to its hexadecimal equivalent number.
 - Convert $(177.25)_{10}$ to octal. (b)
 - Using 7's complement and 8's complement, obtain the difference: (c) 1023₈ - 424₈.

$$4 + 3 + 5 = 12$$

Group - C

- Reduce the following Boolean expression into four literals and draw 4. (a) the diagram using minimum number of NAND gates: (A+C+D)(A+C+D')(A+C'+D)(A+B').
 - Simplify the Boolean function (b) $F(w,x,y,z)=\Sigma(1,3,7,11,15)$ with don't care conditions $d(w,x,y,z)=\Sigma(0,2,5)$. 2

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What is the difference between K-Map and Quine McClusky's Method?

Simplify the following Boolean Function by Quine McClusky's method (c) $F=\Sigma(0,1,2,8,10,11,14,15).$

4 + (3+1) + 4 = 12

- 5. (a) Prove that the sum of minterms of a Boolean function of n variables is equal to 1.
 - (b) Express the following as the POS form that is in the form of product of minterms: F(A,B,C,D)=D(A'+B)+B'D.

6 + 6 = 12

Group - D

- Draw the Diagram of BCD to excess-3 Code Converter with 6. (a) explanation.
 - Implement a Full adder with a Decoder and two OR Gates. (b)
 - (c) Show that a 4 x 16 decoder can be constructed with two 3 x 8 decoders. 4 + 4 + 4 = 12
- 7. (a) Design a 4:1 multiplexer using 2:1 multiplexer.
 - (b) Design a 8 to 1 multiplexer by using the four variable function given by $F(A,B,C,D) = \sum m(0,1,3,4,8,9,15).$

5 + 7 = 12

Group - E

8. (a) Design a sequential circuit whose state-table is listed below:

Prese	nt State	Input	Next	State	Output
A1	A2	Х	A1	A2	У
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

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(b) Convert a JK flip-flop to a D flip-flop. You can use additional circuitry if required.

6 + 6 = 12

- 9. (a) What is the difference between synchronous counter and asynchronous counter?
 - (b) What is a shift register? Can a shift register be used as a counter? If yes, explain how?
 - (c) With relevant diagram explain the working of a master-slave JK flip flop.

3 + 3 + 6 = 12

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DIGITAL LOGIC DESIGN (MCAP 1101)

Time Allotted : 3 hrs

1.

Full Marks : 70

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and <u>any 5 (five)</u> from Group B to E, taking <u>at least one</u> from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A (Multiple Choice Type Questions)

Choose	$10 \times 1 = 10$			
(i)	Find the unknown (a) 6	base x from the rela (b) 3	ation (110101) ₂ = (c) 4	: (311) _x (d) 5.
(ii)	Find the Grey Code (a) 1010	e for decimal 12 (b) 1100	(c) 0110	(d) 1001.
(iii)	When signed num of the following r zero? (a) Sign-magnitud (c) 2's complement	bers are used in bin notations would ha e t	ary arithmetic, th ave unique repro (b) 1's comp (d) 9's comp	nen which one esentation for lement lement.
(iv)	Floating point representation is the combination of(a) integer and fraction(b) mantisa and exponent(c) long integer and double(d) integer and double.			and exponent nd double.
(v)	How many Flip-Flo (a) 5	ops are required for (b) 6	mod–16 counter (c) 3	? (d) 4.
(vi)	Which of the follow (a) S=0, R=0 (c) S=1, R=0	ing input combination	ns is not allowed in (b) S=0, R=1 (d) S=1, R=1.	n SR flip-flop?
(vii)	Data can be change (a) shift registers (c) combinational	ed from special code circuits	e to temporal cod (b) counters (d) A/D conv	e by using verters.

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