DIGITAL SYSTEMS DESIGN
(ECEN 2002)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) The race-around condition does not occur in flip-flop
(a) J-K (b) Master slave (c) T (d) None of these.

(ii) The output of a gate is low if and only if all its inputs are high. It is true for
(a) AND (b) XNOR (c) NOR (d) NAND

(iii) What will be the octal equivalent of $(10001111.101101)_2$?
(a) $(215.66)_8$ (b) $(217.55)_8$ (c) $(142.65)_8$ (d) $(515.76)_8$.

(iv) What is the minimum number of NAND gates required to realize XOR gate?
(a) 3 (b) 4 (c) 5 (d) 6.

(v) How many full adders are required to make n-bit parallel adder?
(a) n (b) n+1 (c) n-1 (d) n/2.

(vi) How many flip flops are required to design a mod-10 counter?
(a) 3 (b) 4 (c) 5 (d) 6.

(vii) A system has following negative numbers stored in 2's complement binary form as shown. The wrongly stored number is
(a) -32 as 11100000 (b) -37 as 11011011
(c) -48 as 11101000 (d) -89 as 10100111

(viii) The base of the number system for the addition operation 24+14=41 to be true is
(a) 8 (b) 7 (c) 6 (d) 5.

(ix) The number of select lines required in a single input and 256 output DEMUX is
(a) 8 (b) 16 (c) 32 (d) 64

(x) A universal register
(a) accepts serial input (b) accepts parallel input
(c) gives serial and parallel outputs (d) is capable of all of the above.

Fill in the blanks with the correct word

(xi) If in a parallel counter, t_{pd} for each FF is 50ns and t_{pd} for each AND gate is 20ns the f_{max} will be _____.

(xii) The logic family that dissipates minimum power is _____.

(xiii) A mod-2 counter followed by a mod-5 counter is _____ counter.

(xiv) A 10-bit DAC provides an analog output having maximum value of 10.23 volts. Resolution of the DAC is _____.

(xv) The memory which is ultraviolet erasable and electrically programmable is _____.

Group - B

2. (a) Realise Y=(A+C)(A+D')(A+B+C') using NOR gates only. *[(CO1)(Analyse/HOCQ)]*
   (b) Perform (39)-(22) using 2's complement method. *[(CO1)(Analyse/HOCQ)]*
   (c) Perform BCD addition of $(592)_{BCD}$ +$(754)_{BCD}$. *[(CO1)(Analyse/HOCQ)]*

4 + 4 + 4 = 12

3. (a) Minimize the Boolean function and realize using NAND gates only
   $F(A, B, C, D) = \sum m(2,3,8,10,11,12,14,15) + \sum d(0,1)$. *[(CO1)(Apply/IOCQ)]*
   (b) Minimize the Boolean function using tabular method
   $F(A, B, C, D) = \sum m(0,1,2,6,8,9)$. *[(CO4)(Remember/LOCQ)]*

6 + 6 = 12

Group - C

4. (a) Design a full substractor using half substractor module and necessary logic gates. *[(CO2)(Apply/IOCQ)]*
   (b) Design a BCD to excess-3 code converter circuit. *[(CO2)(Evaluate/HOCQ)]*

6 + 6 = 12

5. (a) Design MOD-3 synchronous UP counter using JK flip flop. *[(CO3)(Create/HOCQ)]*
   (b) Design a 4 bit parallel in serial out shift register. *[(CO3)(Create/HOCQ)]*

6 + 6 = 12

Group - D

6. (a) What is the advantage of J-K flip-flop over S-R flip-flop? *[(CO3)(Understand/LOCQ)]*
   (b) Write the truth table, state table, excitation table and hence derive the chracteristics equation of J-K flip-flop. *[(CO3)(Analyze/HOCQ)]*
   (c) Realize D flip-flop using J-K flip-flop. *[(CO3)(Apply/IOCQ)]*

2 + 6 + 4 = 12

7. (a) Explain the operation of successive approximation type ADC with circuit diagram. *[(CO4)(Apply/IOCQ)]*

(b) Construct a R-2R ladder DAC and explain briefly the operation.

[(CO4)(Remember/LOCQ)]

6 + 6 = 12

Group - E

8. (a) Implement the logic function $f = A\bar{B} + \bar{A}B$ using CMOS logic. *[(CO5)(Apply/IOCQ)]*

   (b) Realise a two input NAND gate using CMOS logic. *[(CO5)(Apply/IOCQ)]*

6 + 6 = 12

9. Write short notes on any three: **(3 × 4) = 12**

   (i) EPROM

   (ii) TTL NAND Gate

   (iii) CMOS NOR gate

   (iv) Universal Gates

   (v) D Morgans Theorem. *[(CO4)(Apply/IOCQ)]*

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	14.58	47.92	37.5

Course Outcome (CO):

After the completion of the course students will be able to

1. Make use of the concept of Boolean algebra to minimize logic expressions by the algebraic method, K-map method, and Tabular method.
2. Construct different Combinational circuits like Adder, Subtractor, Multiplexer, De-Multiplexer, Decoder, Encoder, etc.
3. Design various types of Registers and Counters Circuits using Flip-Flops (Synchronous, Asynchronous, Irregular, Cascaded, Ring, Johnson).
4. Outline the concept of different types of A/D and D/A conversion techniques.
5. Realize basic gates using RTL, DTL, TTL, ECL, and CMOS logic families.
6. Relate the concept of Flip flops to analyze different memory systems including RAM, ROM, EPROM, EEROM, etc.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*