ANALOG VLSI DESIGN
(ECEN 4145)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) For push-pull amplifier operation
(a) NMOS will be in saturation, PMOS will be in linear mode
(b) NMOS will be in linear, PMOS will be in saturation mode
(c) Both NMOS and PMOS will be in saturation mode
(d) Both NMOS and PMOS will be in linear mode.

(ii) An ideal differential amplifier amplifier should have CMRR
(a) 0 < CMRR < 1 (b) 1
(c) Infinite (d) Zero.

(iii) If the substrate terminals of the transistors forming the source-coupled pair of the CMOS differential amplifier is connected to ground then,
(a) Threshold voltages depend on C_{bd} and C_{bs}
(b) Threshold voltages decrease nonlinearly
(c) Threshold voltages decrease linearly
(d) Threshold voltages increase.

(iv) Practical current mirror circuits deviate from the ideal behaviour due to
(a) Channel length modulation effect
(b) Threshold voltage offset between two transistors
(c) Imperfect geometrical matching
(d) all of the above.

(v) Linear Region of Ideal MOS Transistor can be modelled as
(a) Capacitance (b) Resistance
(c) Voltage Source (d) Current Source.

(vi) Most Popular Scaling Technique in Today's Nano Technology is
(a) Constant Voltage Scaling (b) Constant Energy Scaling
(c) Constant Charge Scaling (d) Constant Field Scaling.

(vii) A MOSFET is ensured to operate in saturation region when
(a) Gate-source shorted (b) Gate-substrate shorted
(c) Source-substrate shorted (d) Gate-drain shorted.

(viii) 3D Transistor is created using below Fabrication Process
(a) FINFET (b) SOI
(c) NMOS Bulk CMOS (d) PMOS Bulk CMOS.

(ix) The frequency of the signal applied to the switched-capacitor circuit should satisfy the criteria
(a) $f_{signal} << f_{clock}$ (b) $f_{signal} >> f_{clock}$
(c) $f_{signal} = 2f_{clock}$ (d) $f_{signal} = 0.5f_{clock}$.

(x) 0.7 Technology Scaling enables Layout area scaling of
(a) 0.49 (b) 1.0 (c) 1.42 (d) 0.65.

Fill in the blanks with the correct word

(xi) Full Form of PTAT is _____.

(xii) Full Form of SOI is _____.

(xiii) The process of pattern transfer through mask is known as _____.

(xiv) One of the limitations of the MOS switch is given by _____ injection.

(xv) For the n-channel enhancement type MOSFET, the substrate terminal is connected to the most _____ potential.

Group - B

2. (a) Briefly explain the "channel formation" in *n*-channel enhancement-type MOSFET with necessary diagram. *[(CO1)(Understand/LOCQ)]*
(b) An ideal *n-channel* MOSFET has the following parameters:
$L = 1.3\mu m$; $\mu_n = 660cm^2/V.s$; $C_{OX} = 7\times10^{-8}\ F/Cm^2$; $V_T = 0.66V$; What should be the channel width (W) such that $I_{D(sat)} = 5mA$ for $V_{GS} = 5V$? *[(CO1)(Evaluate/HOCQ)]*
(c) Do you find the supply voltage of *+1.8V* to be suitable for both *180nm and 45nm* technology node? Justify your answer. *[(CO2)(Apply/IOCQ)]*
4 + 5 + 3 = 12

3. (a) Briefly explain the short-channel effects in MOS structure. *[(CO2)(Understand/LOCQ)]*
(b) Derive the expression of drain current in MOS device and draw the characteristics curve. *[(CO1)(Apply/IOCQ)]*
(c) Distinguish between the transfer characteristics of depletion-type and enhancement-type MOSFET. *[(CO1)(Apply/IOCQ)]*
5 + 4 + 3 = 12

Group - C

4. (a) How you will use Photo Lithography using Negative Photo-resist to create N+ Diffusion in a P Type Substrate? *[(CO3)(Analyze/IOCQ)]*

(b) Explain the difference between Wet Oxidation Dry Oxidation. *[(CO3)(Analyze/IOCQ)]*

(c) Explain the difference between Lambda and Micron Rules. *[(CO3)(Analyze/IOCQ)]*

6 + 3 + 3 = 12

5. (a) Explain CMOS Fabrication flow step by step using self aligned N-Well Process Techniques. *[(CO3)(Analyze/IOCQ)]*

(b) Explain Structure of FINFET Transistor. *[(CO3)(Analyze/IOCQ)]*

(c) Explain Common Centroid Layout using an example. *[(CO3)(Analyze/IOCQ)]*

6 + 3 + 3 = 12

Group - D

6. (a) Briefly explain the operation of MOS as a switch. *[(CO4)(Understand/LOCQ)]*

(b) Can a "Dummy Transistor" help in charge injection cancellation? Justify your answer including the reason behind the name "dummy". *[(CO4)(Apply/IOCQ)]*

(c) Determine the region of operation of the MOSFET in *Fig. 1* and write the relevant expression of channel resistance. *[(CO4)(Apply/IOCQ)]*

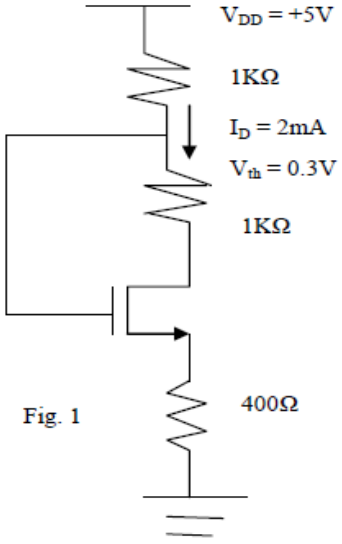

Fig. 1

4 + 3 + 5 = 12

7. (a) Explain Small Signal low frequency model for NMOS. *[(CO4)(Analyze/IOCQ)]*

(b) Evaluate how Diode AC resistance is dependent on NMOS transconductance when the NMOS is used as diode. *[(CO4)(Evaluate/HOCQ)]*

(c) Evaluate how $V_{DD}/2$ can be realized using NMOS based Supply Voltage (V_{DD}) Divider Circuit. *[(CO4)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

Group - E

8. (a) Evaluate how Basic Current Mirror Circuit can be Designed as Current Multiplier where $I_{out}/I_{in} = 4$. *[(CO4)(Evaluate/HOCQ)]*

(b) Evaluate how Cascode Current Sink can increase Output Resistance. *[(CO4)(Evaluate/HOCQ)]*

(c) Explain CMOS bandgap reference circuit. *[(CO4)(Analyse/IOCQ)]*

4 + 4 + 4 = 12

9. (a) Mention the few disadvantages of the switched-capacitor circuits. *[(CO6)(Remember/LOCQ)]*

(b) Emulate the resistor equivalent of series-parallel switched-capacitor circuit. *[(CO6)(Apply/IOCQ)]*

(c) Analyze the accuracy of the switched-capacitor circuits. *[(CO6)(Analyze/IOCQ)]*

4 + 5 + 3 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	17.71	60.42	21.87

Course Outcome (CO):

After the completion of the course students will be able to

ECEN4145.1. Understand the fundamentals of MOSFET device physics

ECEN4145.2. Correlate the fundamental understanding with the evolving VLSI design trends and challenges

ECEN4145.3. Understand the IC fabrication process flow leading to the practical realization of the scaled MOSFETs

ECEN4145.4. Analyze MOS-based analog VLSI sub-circuits and design them, namely, current mirrors, voltage & current references.

ECEN4145.5. Design MOS circuits of practical importance e.g. common-source amplifiers and differential amplifiers.

ECEN4145.6. Understand and apply the knowledge of analog sampled data circuits to synthesize practical circuits such as switched-capacitor filters.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*