M.TECH/VLSI/2ND SEM/VLSI 5241/2015
2015

Low Power VLSI Circuit and System
(VLSI 5241)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 x 1=10**

(i) If Threshold Voltage of transistor is doubled, Dynamic power of Digital Gate
- (a) is doubled (b) is halved
- (c) remains the same (d) increases by a factor of 4.

(ii) If Threshold Voltage of transistor is increased, Channel Leakage of transistor
- (a) increases linearly (b) decreases linearly
- (c) decreases exponentially (d) remains same.

(iii) If Channel Length of transistor is doubled, Channel Leakage of transistor
- (a) is doubled (b) is halved
- (c) remains the same (d) increases by a factor of 4.

(iv) If Channel Length of driver transistor is doubled, delay of Digital Gate
- (a) is doubled (b) is halved
- (c) remains the same (d) increases by a factor of 4.

(v) Memory Cell with Maximum leakage is
- (a) DRAM Cell (b) SRAM Cell
- (c) Latch Cell (d) Flip Flop Cell.

(vi) Maximum Leakage reduction in ROM array is possible with
- (a) All '0' bits in array (b) All '1' bits in array
- (c) 50% '0' bits in array (d) Not dependent on '0' or '1' bits.

(vii) If P_A is Signal Probability of A input of Inverter, the Signal Probability of Inverter Output is
- (a) P_A (b) $1- P_A$
- (c) 1 (d) 0.

(viii) If Keeper Size of Dynamic Gate is increased
- (a) delay increases (b) noise increases
- (c) there is no change in delay (d) there is no change in noise.

(ix) If Rise Time of input of a inverter is increased, then Short Circuit Current
(a) increases linearly (b) decreases linearly
(c) remains same (d) decreases exponentially.

(x) Both Power and Delay Reduction for a Digital Gate is possible if
(a) C_L decreases (b) V_{DD} decreases
(c) Activity Factor decreases (d) C_L increases. .

Group – B

2.(a) If P_A and P_B are Signal Probability of A and B input of a NAND gate, calculate Transition Probability of output Y of NAND gate.

(a) Explain Glitch Power of a Digital Circuit with an example and show how that can be reduced with same example.

6+6=12

3.(a) Under what input condition Channel Leakage Power through a 3 input NAND Gate is minimum and why ?

(b) Draw Gate Delay vs Threshold voltage curve for various Supply Voltage of a digital Gate and explain.

6+6=12

Group – C

4.(a) Explain Dynamic Voltage Scaling (DVS).

(b) Explain Clock Gating.

6+6 = 12

5.(a) What are various components of Switching Load Capacitance (C_L) in Digital Circuit?

(b) What are various techniques of reducing C_L ?

6+6=12

Group – D

6.(a) Why High K plus Metal gate Transistor was introduced from 45nm onwards?

(b) How FINFET can save more channel and gate leakage with respect to traditional MOS Transistor for similar performance?

6+6 = 12

7.(a) For 2 input NOR gate, mention leaking transistors (channel leakage) for all possible combination of inputs. For 3 input NOR gate, mention leaking transistors (channel leakage) for all possible combination of inputs including stacking effect.

6+6 = 12

Group – E

8.(a) Under what condition Dynamic logic gates can provide less power with respect to Static CMOS gates? Explain with example?

(b) How Power reduction is possible from 3 Transistor DRAM cell array to 1 Transistor DRAM cell array? Explain with circuit diagram.

6+6= 12

9.(a) Why Latch based Sense Amplifier consumes less power than Differential pair based Sense Amplifier in SRAM chip? Explain with circuit diagram.

(b) How Feed forward inverter in Keeper Circuit can save power of a dynamic logic gate?

6+6= 12