MICROPROCESSORS AND MICROCONTROLLERS
(ECEN 3104)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) BCD addition in 8085 microprocessor can be performed by which of the following instruction?
(a) DAA (b) LXI (c) LDA (d) LHLD.

(ii) Demultiplexing of address bus is made possible through
(a) ALE pin (b) HOLD pin (c) INTA pin (d) RESET IN pin.

(iii) If the content of accumulator (A←93H) when compared with the content of L register (L←A4H), which of the following flag bits reflect the correct status?
(a) Carry flag is set and Zero flag is reset
(b) Carry flag is reset and zero flag is set
(c) Carry and Zero flags are reset
(d) Carry and Zero flags are set.

(iv) Which of the following will be the content of DE register pair if DCX D is executed assuming the above register pair contains 2000H?
(a) DE←20FFH (b) DE←2FFFH (c) DE←10FFH (d) DE←1FFFH.

(v) Calculate the address lines required for an 8K-byte (1024 x 8 = 8192 registers) memory chip?
(a) 11 (b) 12 (c) 13 (d) 14.

(vi) The control word in control register in 8255A specifies
(a) an I/O function of each port (b) input and output data of each port
(c) accessibility of each port (d) all of (a), (b) & (c).

(vii) In 8259A the function of enabling or disabling individual interrupt request inputs is performed by
(a) IRR (b) ISR (c) IMR (d) Priority resolver.

(viii) Which of the following is an example of branch instruction?
(a) XRI 13H (b) JC 2025H (c) LDAX B (d) LXI B, 2053H.

(ix) Which of the following are the two 16-bit SFRs of 8051 microcontroller?
(a) PC, DPTR (b) SP, PSW (c) SP, DPTR (d) PC, SP.

(x) The instruction MOV AX, [BX] is an example of
(a)Register Indirect addressing (b) Indexed addressing
(c) Direct addressing (d) Based addressing.

Fill in the blanks with the correct word

(xi) _____ is defined as one subdivision of the operation performed in one clock period.

(xii) _____ is a status signal used to differentiate between I/O and memory operations.

(xiii) _____ is a non- maskable interrupt and has the highest priority.

(xiv) STA 2050H is a _____ byte instruction.

(xv) _____ pin is used for Direct Memory Access transfer in 8085.

Group - B

2. (a) Starting with the memory address 8000H.

Line No	Mnemonics
1	MVI A, 23H
2	RRC
3	MOV C, A
4	HLT

(i) At line 2, write the content of accumulator and carry after RRC instruction?
(ii) Define the instruction word size of MVI A, 23H?
(iii) Name the addressing mode of MOV C, A? *[(CO1)(Remember/LOCQ)]*

(b) Assume 03H and 81H data are stored in A and H registers respectively. Show the content of accumulator after ORA operation is performed. Also show the flag bits S, Z, P and CY. *[(CO1)(Apply/IOCQ)]*

(c) Calculate the number of memory chips needed to design 8K-byte memory if the memory chip size is 1024 × 1. *[(CO1)(Analyze/IOCQ)]*

(2 + 1 + 1) + 5 + 3 = 12

3. (a) Which instruction is used for masking operation? Register A contains 8FH. Write an instruction to remove the lower order 4 bits of register A through masking operation. Find out the status of the Zero and Sign flag after the operation. *[(CO2)(Evaluate/HOCQ)]*

(b) Define addressing modes? How many addressing modes are there in 8085? *[(CO2)(Understand/LOCQ)]*

(c) Explain the function of Ready and ALE pin. *[(CO1)(Understand/LOCQ)]*

3 + (1 + 2) + 6 = 12

Group - C

4. (a) Compare Push & POP and CALL & Return instructions. *[(CO3)(Analysis/IOCQ)]*
   (b) Assuming the microprocessor is completing an RST 7.5 interrupt request, check to see if RST 6.5 is pending. If it is pending enable RST 6.5 without affecting any other interrupts, otherwise return to main program. Design an ALP accordingly. *[(CO3)(Design/HOCQ)]*
   (c) Explain with an example how a physical address can be generated from a segment address in 8086? *[(CO4)(Understand/LOCQ)]*

4 + 4 + 4 = 12

5. (a) Design the ALP along with the flowchart to transfer the entire block of data to new memory locations starting from 8000H. Assume 16 bytes of data are stored in memory locations starting from 9050H to 905FH. Write the output in hex code along with corresponding memory locations where the data will be stored. *[(CO3)(Design/HOCQ)]*
   (b) Discuss in details about the interpretation of the accumulator bit pattern for SIM instruction. *[(CO3)(Understand/LOCQ)]*
   (c) Describe the function of three flags of control flag register of 8086 microprocessor. *[(CO4)(Remember/LOCQ)]*

6 + 3 + 3 = 12

Group - D

6. (a) Which peripheral is designed to mange 8 interrupts and is compatible with 8085 and 8086. List the different types of functions performed by this peripheral. *[(CO5)(Remember/LOCQ)]*
   (b) How many modes of operation are there in 8255A? *[(CO5)(Remember/LOCQ)]*
   (c) Design a BSR control word subroutine to set bits PC_7 & PC_3 and reset them after 10ms for 8255A. Assume that a delay subroutine is available. Consider the address of the control register to be 83H. *[(CO5)(Design/HOCQ)]*

(1 + 5) + 2 + 4 = 12

7. (a) Discuss about the functions of interrupt registers and priority resolver of 8259A programmable interrupt controller. *[(CO5)(Understand/LOCQ)]*
   (b) For 8255A, identify the Mode 0 control word to configure port A and port C_u as input ports and port B and port C_L as output ports for I/O mode? *[(CO5)(Understand/LOCQ)]*
   (c) Explain the function of ICWs and OCWs of 8259A interrupt controller. *[(CO5)(Understand/LOCQ)]*

4 + 4 + 4 = 12

Group - E

8. (a) Explain the operations of the following instructions of 8051 microcontroller:-
   (i) MOV A, #25H
   (ii) ADD A, R7
   (iii) MOV R0, 40H. *[(CO6)(Evaluate/HOCQ)]*

(b) Define register indirect addressing mode and indexed addressing mode. Give one example for each of them. *[(CO6) (Understand/LOCQ)]*

(c) Discuss the PSW of 8051 microcontroller. *[(CO6) (Understand/LOCQ)]*

(1 + 1 + 1) + (2 + 2) + 5 = 12

9. (a) Show the status of CY and P flags after the addition of 9CH and 64H in the following instructions. Also show the content of A.

MOV A, #9CH

ADD A, #64H. *[(CO6)(Apply/IOCQ)]*

(b) Explain the interrupts of 8051 microcontroller. *[(CO6)(Evaluate/HOCQ)]*

(c) Write one advantage and disadvantage of register indirect addressing mode. *[(CO6)(Apply/IOCQ)]*

4 + 5 + 3 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	54.17	19.79	26.04

Course Outcome (CO):

After the completion of the course students will be able to

1. Demonstrate the knowledge of Digital Electronics with learning of the microprocessor and microcontroller.
2. Develop the concepts of CPU, timing and control signals I/O devices, and various BUS structure.
3. Learn about interrupts, stack and subroutine and write ALPs for given problems with flowcharts.
4. Conceptualize the architecture of 8086 family & ARM basics along with its parallel application.
5. Understand interfacing of processor with memory and I/O devices and analyze their problems.
6. Analyze microcontroller 8051 architecture in terms of Ports, Memory, Counters and Timers.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*