2015

Analog IC Design

(VLSI 5203)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and

any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 x 1=10**

(i) Switched capacitor circuits are

1. discrete in amplitude and discrete in time
2. discrete in amplitude and continuous in time

(c) continuous in amplitude and continuous in time

(d) continuous in amplitude and discrete in time.

(ii) The PSRR of the op-amp is given by,

(a)  (b) 

(c)  (d) none of the above.

(iii) The backgate transconductance (g_{mb}) obtained in the small-signal analysis of the MOSFET depends on

1. body coefficient only (b) back gate bias only

(c) body coefficient and backgate bias both (d) none of the above.

(iv) The gate-to-channel capacitance of the MOSFET is given as,

(a) $C_{GC} = W_{eff}(L\text{-}LD)C_{ox}$ (b) $C_{GC} = W_{eff}(L\text{-}LD)C_{ox}$

(c) $C_{GC} = W_{eff}(L+LD)C_{ox}$ (d) $C_{GC} = W_{eff}LC_{ox}$.

(Where, LD stands for the lateral diffusion component.)

(v) An ideal differential amplifier should have common mode voltage gain,

(a) $A_{VC} = 0$ (b) $A_{VC} = 1$ (c) $A_{VC} = \infty$ (d) $0 < A_{VC} < 1$.

(vi) RMS quantization noise of a ADC can be given by (if the quantization level is 'q')

(a) $q/12$ (b) $q^{1/2}$ (c) $q/12^{1/2}$ (d) $q/2$.

(vii) SFDR is the specification for

(a) ADC (b) DAC

(c) both ADC and DAC (d) all RFIC.

(viii) Assuming that the transfer characteristic of a converter is given by

D= K+GA, and considering K=0 the type of converter would be

(a) Bipolar converter (b) sign magnitude converter

(c) Uniplar converter (d) BCD converter.

(ix) For a RF mixer conversion gain is having the unit of

(a) current (b) voltage

(c) conductance (d) resistance.

(x) In CMOS RFIC noise figure can be expressed in terms of

(a) quality factor (b) noise factor

(c) conductance (d) resistance.

Group – B

2.(a) Obtain the small-signal model of the MOS transistor from the dc model and explain the small-signal equivalent circuit for the MOSFET including the parasitic capacitors.

(b) Explain the model of a non-ideal MOS switch.

6+6=12

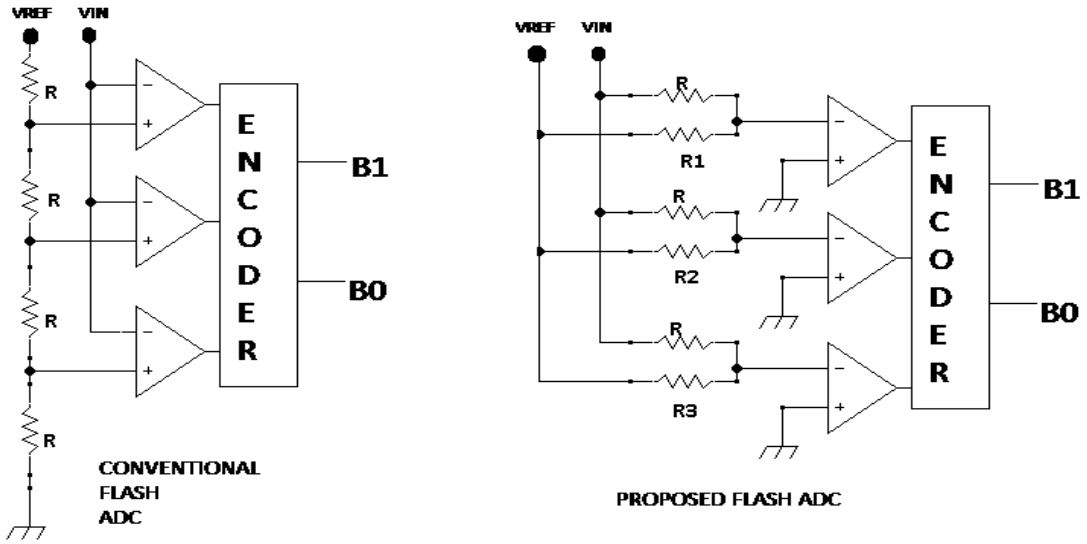
3.(a) Draw the circuit and current-voltage characteristics of a simple MOS current sink. Calculate the small-signal output resistance for this simple current sink if I_{out}=100 μA and channel length modulation parameter λ = 0.04 V^{-1}. Evaluate the differential transconductance of the CMOS differential amplifier using NMOS transistors from the large signal analysis.

2. Explain the circuit operation of a CMOS differential amplifier using a current mirror load with the help of large signal analysis.

(2+2+4)+4=12

Group – C

4.(a)



Two versions of a 2-bit flash ADC are shown in the figure shown in page 2. Design R1, R2, R3 to make the proposed ADC equivalent to the conventional ADC. Compare the performance, advantages and disadvantages between the two ADCs.

(b) Explain the working principle of a voltage scaled DAC. Derive the expressions for INL and DNL assuming the worst case.

6+(3+3)=12

5.(a) Classify DC errors of data converters and explain.

(b) Find the expression for ENOB. State the effect of aperture jitter noise on SNR of a ADC with proper diagrams.

7+(2+3)=12

Group – D

6.(a) Compare the bandwidth estimation techniques for RF circuits

(b) Draw the layouts for square, octagonal, hexagonal, circular and spiral inductors. Give the mathematical equivalent expression for a rectangular shaped inductor.

6+(3+3)=12

7.(a) Explain the working principle of a single ended LNA.

(b) Discuss how the shortcomings of a single ended LNA can be overcome by using a suitable architecture.

7+5=12

Group – E

8.(a) Explain why a single common-source stage does not oscillate if it is placed in a unity gain loop. What is the requirement of the third inverting stage in a three-stage ring oscillator?

(b) Calculate the oscillation frequency and minimum voltage gain per stage of a three-stage ring oscillator.

(2+6)+4=12

9.(a) Mention the advantages of the switched capacitor circuits. Draw the configuration of a parallel switched capacitor equivalent resistor and emulate the equivalent resistor in terms of the capacitor and the period of the clock waveform.

(b) For this configuration, find out the capacitor C that can emulate a 1 MΩ resistor if the clock frequency is 100 KHz.

(2+6)+4=12