M.TECH/VLSI/2ND SEM/VLSI 5201/2015
2015

VLSI Processor Architecture
(VLSI 5201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following: **10 x 1=10**

(i) Micro-instructions are kept in
(a) Main memory (b) Control memory
(c) Cache memory (d) flash memory.

(ii) The component that works together with a processor and execute key functions much faster than processor is known as
(a) coprocessor (b) multiprocessor
(c) control units (d) accelerator.

(iii) The Second stage of pipelining is
(a) Instruction fetch (b) Instruction decode
(c) execute (d) None.

(iv) In a microprocessor the address of the next instruction to be executed is stored in
(a) Stack Pointer (b) Instruction Pointer
(c) Program Counter (d) Status Register.

(v) VLIW instructions are used in
(a) Multithread Processor (b) superscalar
(c) co processor (d) none.

(vi) The TMS320CX DSPs are said to have advanced Harvard architecture because they have
(a) separate memory bus structure for program and data
(b) instructions enabling data transfer between the program and data memory
(c) same bus for program and data
(d) program and data memory which is non overlapping

(vii) Instructions ADD a_1, a_2, a_3
SUB a_4, a_5, a_1
It is an example of
(a) WAW (b) RAR (c) RAW (d) WAR hazard

(viii) The central ALU of TMS320CX processor has _____ bit ALU and one of the operands for the ALU operation comes from _____.

(a) 32, ACC (b) 16, ACC
(c) 32, ACCB (d) 16, ACCB.

(ix) Hardware accelerators are

(a) built inside ALU
(b) application specific and demonstrates orders of magnitude in efficiency
(c) Used for gaming only
(d) Ecommerce specific.

(x) Multi – core superscalar processor is a?

(a) SISD (b) SIMD (c) MIMD (d) MISD.

Group – B

2.(a) Distinguish between computer architecture and organization. Compare Harvard, Von Neumann and Modified Harvard Architecture and illustrate these architecture using block diagram?

(b) Give the differences between CISC, RISC and VLIW architectures. Illustrate the instruction sets for CISC and RISC and VLIW with suitable examples.

(2+4)+(4+2)=12

3.(a) What do you mean by instruction set architecture? Give the differences between vector and scalar architectures.

(b) Define the Flynn's taxonomy. Illustrate the four classification of Flynn's taxonomy.

(1+4)+(1+6)=12

Group – C

4.(a) What do you mean by the control unit? Draw the block diagram of the hard wired control unit and micro programmed control unit.

(b) Why was micro programming preferred on many old processors (earlier) and why do modern processors mostly follow hardwired control?

(2+4)+6=12

5.(a) What do you mean by pipeline? What are the limits on how much a processor's performance can be improved with the help of pipelining?

(b) What are microcontrollers? How microprocessor differs from SOC and board-level design?

(2+4)+(2+4)=12

Group – D

6.(a) What are the differences between scalar and vector pipelining? Explain using block diagram superscalar architecture for parallel processing.

(b) Illustrate the execution of two instruction ADD R_1, R2, R_3 and SUB R_4, R_1, R5 using the pipeline technique. Why does bypassing usually eliminate or reduce stalls due to data dependencies but has no effect on stalls due to control hazards?

(3+3)+(3+3)=12

7.(a) Compare the fixed point and floating point DSP processor. Give the characteristics of the TMS320C54xx digital signal processor and illustrate the functional blocks of this processor.

(b) Describe the function of ALU, barrel shifter, CSSU units of digital signal processor TMS320C54xx.

(2+4)+(2+2+2)=12

Group – E

8.(a) Define the ARM processor and give the special features of this processor. Explain the software interrupt, data processing, data transfer, swap, multiply, THUMB and branching instructions used in ARM processors.

(b) Draw the block diagram of ARM processor. What do you mean by course-grain parallelism?

(1+2+3)+(4+2)=12

9.(a) What is the difference between multiprocessors and multithreaded processors? Describe accelerators.

(b) What do you mean by SOC design? What are the benefits of processor customization?

(4+2)+(3+3)=12