M.TECH/VLSI/2ND SEM/VLSI 5202/2015
2015

VLSI Design, Verification and Testing
(VLSI 5202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 x 1=10**

(i) In which of the following Memory array Periodic Refresh is needed?
(a) ROM (b) Register File (c) DRAM (d) SRAM.

(ii) Which memory can hold the bit value when there is no power supply?
(a) SRAM (b) ROM (c) DRAM (d) Register File.

(iii) Memory with multiple read and write port is
(a) SRAM (b) ROM (c) Register File (d) DRAM.

(iv) For modern process, Wire Aspect Ratio (t/w) is
(a) 1 (b) 2 (c) 3 (d) 4.

(v) Wire RC model acts as
(a) Low pass filter (b) High pass filter
(c) Band pass filter (d) All pass filter.

(vi) Transistor performs slowest at
(a) High Voltage, High Temperature (b) High Voltage, Low Temperature
(c) Low Voltage, High Temperature (d) Low Voltage, Low Temperature.

(vii) ATPG is based on
(a) Stuck at fault (b) DFT (c) Bridging fault (d) BIST.

(viii) Signature analyser (SA) is part of
(a) Scan Design (b) Boundary Scan (c) BIST (d) Ad hoc DFT.

(ix) Hold margin for a path is +20ps for Cycle Time of 200ps. If Cycle time is reduced to 180ps, then new hold margin for the path will be
(a) +40ps (b) +20ps (c) 0ps (d) -20ps.

(x) Yield Y = 99% and Fault Coverage T = 90%, DPM (Defects Per Million) is
(a) 1000 (b) 10,000 (c) 28,000 (d) 50,000.

Group – B

2.(a) Explain various components of a Memory Block with Diagram.

(b) For a Memory Block of 4K Memory Locations and 16 Data bits, Explain how many row address bits and how many column address bits are needed.

6+6=12

3.(a) Explain write '1' followed by read '1' operation in 1-Transistor DRAM Circuit using circuit diagram and timing waveforms.

(b) Explain sizing criteria of 6 Transistor SRAM cell.

6+6=12

Group – C

4.(a) Explain difference between differential Pair Sense Amplifier vs Latch based Sense Amplifier with circuit diagram

(b) What is best circuit scheme to create 5 to 32 bit decoder? Explain with diagram.

6+6=12

5.(a) As per Process Technology, Metal-8 resistance is 100mohms/um and capacitance is 0.2ff/um. If 1mm wire is routed using Metal-8, draw circuit diagram of 3 segment pi model with appropriate resistance and capacitance value of individual segments.

(b) Why driver side of a wire needs to be low resistance and receiver side of the wire needs to be low capacitance, explain using Elmore Delay model?

6+6=12

Group – D

6.(a) For a flip flop based sequential circuit, Cycle Time = 200ps, Setup Time = 30ps, Clock-Skew = 20ps, Combinational Delay = 60ps, Clock to Out Delay of Flop = 40ps. Hold Time = 50ps. What is setup margin and hold margin for the Circuit?

(b) What is clock skew and what are sources of Clock Skew?

6+6=12

7.(a) Explain H-Tree of clock distribution using circuit diagram.

(b) Explain transparency of a D-Latch with circuit diagram and timing waveforms.

6+6=12

Group – E

8.(a) What is input test pattern to detect Stuck-at-1 fault at the Output of a 2 input NAND gate ?

(b) Explain D-Algorithm using an example.

6+6=12

9.(a) Draw Circuit diagram of Scan Flip Flop and explain how it works.

(b) Draw block diagram of Scan Design/Structure and explain its operation.

6+6=12