ELECTRONIC DESIGN AUTOMATION
(ECEN 3106)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Moore's law predicts the number of transistors doubles in every
(a) 1 year (b) 2 years
(c) 18 months (d) 6 months.

(ii) Layout design rules specify
(a) Minimum allowable linewidths for physical objects on chip
(b) Minimum feature dimensions
(c) Minimum allowable separations between two such features
(d) All of the above.

(iii) Technology Mapping in logic synthesis is an important task in
(a) Technology dependent optimization
(b) Logic expression optimization only
(c) Expressing netlist using gate layouts from technology library
(d) Both (a) & (c).

(iv) Minimum number of transistors to design a 2-input XOR gate using standard CMOS technology is
(a) 6 (b) 8 (c) 10 (d) 12.

(v) Stick diagram represents
(a) Logic (b) Circuit (c) Layout (d) Architecture.

(vi) In λ-based design rule system, the minimum feature size is taken to be
(a) λ (b) 2λ (c) 3λ (d) λ/2.

(vii) Detailed routing includes
(a) Switchbox routing (b) Channel routing
(c) Both (a) & (b) (d) None of (a), (b) & (c).

(viii) HDL in VLSI stands for
(a) Highly Decipherable Language (b) Hardware Domain Language
(c) Heuristic Description Language (d) Hardware Description Language.

(ix) BDD is a
(a) Cyclic graph (b) Directed tree structure
(c) Block diagram representation (d) None of (a), (b) & (c).

(x) In order to avoid meta-stability problem in clocked *D-Latch*, a valid *D*-input must be stable for
(a) Set up time (b) Hold time
(c) Both (a) & (b) (d) None of (a), (b) & (c).

Fill in the blanks with the correct word

(xi) The transmission gate is a _____ switch.

(xii) Verilog is a case sensitive language. _____ (write 'True' or 'False').

(xiii) RTL synthesis belongs to _____ synthesis part of the EDA flow.

(xiv) The number of transistors required to implement the function (a.b+c)', using CMOS NAND, NOR and Inverter is_____.

(xv) During the physical designing step, the process of dividing an entire VLSI circuit into a number of sub-circuits is called _____.

Group - B

2. (a) Briefly explain the principle of operation of CMOS inverter with necessary circuit diagram. *[(CO2)(Understand/LOCQ)]*

(b) Design a sequential circuit which obeys the following truth table: *[(CO3)(Create/HOCQ)]*

S	***R***	Q_{n+1}	$(Q_{n+1})'$	***Operation***
0	*0*	*1*	*1*	*Not Allowed*
0	*1*	*1*	*0*	*Set*
1	*0*	*0*	*1*	*Reset*
1	*1*	Q_n	$(Q_n)'$	*Hold*

(c) Implement the following combinational logic function using Transmission Gate *(TG)* : *F = AB + A'C' + AB'C.* *[(CO3)(Apply/IOCQ)]*

4 + 5 + 3 = 12

3. (a) Realize a 2X1 MUX using CMOS Transmission Gates. *[(CO3)(Apply/IOCQ)]*

(b) Show how CMOS Transmission Gates may be used to obtain a D-latch circuit. Explain its operation. *[(CO3)(Apply/IOCQ)]*

5 + 7= 12

Group - C

4. (a) Briefly explain the concept of technology node with proper diagram. Can we apply the same supply voltage (say, V_{DD} *= +1.8V*) for both *180nm and 45nm*

technology nodes? Justify your answer with appropriate mathematical reasoning. *[(CO1)(Apply/IOCQ)]*

(b) Mention the key features of standard cell based design methodology. *[(CO1)(Understand/LOCQ)]*

(c) Distinguish between *PAL and PLA*. *[(CO1)(Apply/IOCQ)]*

5 + 4 + 3 = 12

5. (a) Briefly describe the floorplan of *FPGA* with necessary diagram. *[(CO1)(Understand/LOCQ)]*

(b) Implement the following logic function using *AND / OR plane PLA* : *[(CO1)(Apply/IOCQ)]*

F1 = ab
F2 = bc +a'd'
F3 = a'b'c +cd +ac

(c) Mention the key features of full custom design methodology. *[(CO1)(Understand/LOCQ)]*

4 + 5 + 3 = 12

Group - D

6. (a) Briefly explain the high-level synthesis flowchart. *[(CO4)(Understand/LOCQ)]*

(b) Design the data flow graph and then provide the scheduling solution for the operation *"(a*b*c*d)+e"* with highest possible speed of design where maximum *2* multiplications (*) are allowed per cycle of clock. *[(CO4)(Create/HOCQ)]*

(c) Draw the *BDD* for *XOR* function. *[(CO5)(Apply/IOCQ)]*

4 + 5 + 3 = 12

7. (a) State the difference between High Level Synthesis (HLS) and Logic Synthesis of VLSI design. *[(CO4)(Understand/LOCQ)]*

(b) Construct the BDD of the function f=xy+yz+xz for the ordering x<=y<=z. *[(CO4)(Create/HOCQ)]*

(c) Obtain the ROBDD for the same function, f. *[(CO5)(Create/HOCQ)]*

2 + 4 + 6 = 12

Group - E

8. (a) Compare global routing and detailed routing. *[(CO6)(Understand/LOCQ)]*

(b) Draw the Horizontal Constraint Graph (*HCG*) and Vertical Constraint Graph (*VCG*) of the given channel routing problem: *[(CO6)(Create/HOCQ)]*
Upper Boundary : *0BDEBFG0D00*
Lower Boundary : *ACECEAFH0HG*
Here *0* means no connection. Assume, *HV layer (V= Metal 1, H = Metal 2)*

(c) Justify the necessity of different metal layers, if required. *[(CO6)(Apply/IOCQ)]*

4 + 5 + 3 = 12

9. (a) Draw a flow diagram and discuss the physical design steps of VLSI design. *[(CO6)(Remember/LOCQ)]*

(b) Mention the objectives of floor planning. *[(CO6) (Understand/LOCQ)]*

(c) Demonstrate the technique of slicing floor planning with a suitable diagram.

[(CO6)(Apply/IOCQ)]

6 + 2 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	34.38	39.58	26.04

Course Outcome (CO):

After the completion of the course students will be able to

ECEN 3106.1. Getting exposure to VLSI Design Cycle, Process Nodes and Design Challenges
ECEN 3106.2. Designing of Industry Standard CMOS Combinational Digital Gates
ECEN 3106.3. Designing of Industry Standard TG based Sequential Digital Gates
ECEN 3106.4. Learning High Level Synthesis in EDA Flow
ECEN 3106.5. Learning Logic Synthesis in EDA Flow and Verilog RTL.
ECEN 3106.6. Learning Physical Place and Route in EDA Flow.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*