COMPUTER ORGANIZATION AND ARCHITECTURE
(CSBS 2202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Conflict miss can be eliminated, in case of
(a) direct mapping cache (b) fully associative cache
(c) set associative cache (d) can never be eliminated.

(ii) The prefetching is a solution for
(a) data hazard (b) structural hazard
(c) control hazard (d) none of these.

(iii) A computer with cache access time of 40 ns and hit ratio of 0.8 and regular memory has an access time of 100 ns. What is the effective memory access time of CPU?
(a) 52 ns (b) 60 ns (c) 70 ns (d) 80 ns.

(iv) What will be the speed-up for a 4 segment linear pipeline when the number of instructions n = 64?
(a) 4.5 (b) 3.82 (c) 8.16 (d) 2.95.

(v) The technique used to store programs larger than the size of main memory is _____
(a) overlays (b) extension registers
(c) buffers (d) both extension registers and buffers.

(vi) The number of cycles required to complete n tasks with k stage pipeline is
(a) k (b) nk+1 (c) k+n-1 (d) n/k.

(vii) During the transfer of data between the processor and main memory____ is used.
(a) TLB (b) Buffers
(c) Cache memory (d) none of the above

(viii) In Booth's algorithm, for Multiplier = 1000 and Multiplicand = 1100. How many numbers of cycles are required to get the correct multiplication result?
(a) 3 (b) 4 (c) 5 (d) 6.

(ix) Dynamic pipeline allows
(a) multiple functions to evaluate (b) only streamline connection
(c) to perform fixed function (d) none of these

(x) To discard instructions in the pipeline is referred to as
(a) load-use (b) flushing
(c) decoding (d) discarding.

Group - B

2. (a) Prove that, the final carry in carry look ahead adder is dependent only on the carry generated in first adder. *[(CO2)(Analyse/IOCQ)]*
(b) Design a 4-bit serial adder and mark the delay in the circuit. Consider each gate incurs one gate delay. *[(CO2)(Understand/LOCQ)]*

6 + (3 + 3) = 12

3. Evaluate the arithmetic statement X = ((A + B)*(C+D)) / (E*(F – G)) using (i) zero address instructions (ii) one address instructions (iii) two address instructions and (iv) three address instructions. *[(CO3)(Analyse/IOCQ)]*

(3 × 4) = 12

Group - C

4. (a) A computer has a main memory of 64k × 16 and a cache memory of 1k × 2 words. The cache uses direct mapping with block size of four words.
(i) How many bits are there in the tag, index and offset fields of the address format?
(ii) How many bits are there in each word of cache?
(iii) How many blocks can the cache accommodate? *[(CO4)(Apply/IOCQ)]*
(b) Write the expression to calculate average access time for 2-level cache memory and clearly state each term of the expression. *[(CO4)(Apply/IOCQ)]*

(3 + 2 + 2) + 5 = 12

5. (a) For a computer system the page references are 7 0 1 2 0 3 0 4 2 3 0 3 2 and a page table has four frames. Calculate Hit and Miss ratio using FCFS and LRU page replacement algorithm. *[(CO4)(Apply/IOCQ)]*
(b) Let a computer system has cache capacity 64 KB, Main Memory capacity 1 MB, 2 KB page size, pages per set are 2. Show the size & different address fields in direct and set-associative mapping. *[(CO4)(Apply/IOCQ)]*
(c) Compare temporal and spatial locality of reference in memory. *[(CO4)(Understand/HOCQ)]*

(3 + 3) + 4 + 2 = 12

Group - D

6. (a) How can hazard occur in executing the following set of instructions?

I1: MOV R1, A ; [A] <- (R1)
I2: ADD R2, R3; R3 <- (R3) + (R2)
I3: SUB R4, R5; R5 <- (R4) – (R5)
I4: NOP

All the symbols have their usual meanings. You may assume a pipeline unit consisting of four stages. *[(CO5)(Analyse/IOCQ)]*

(b) Prove that K stage linear pipeline can be at most k times faster than that of a non-pipelined serial processor. *[(CO5)(Evaluate/HOCQ)]*

(c) Explain with an example what do you mean by instruction pipeline. *[(CO5)(Understand/LOCQ)]*

6 + 3 + 3 = 12

7. Consider the Reservation Table given below:

	1	2	3	4	5	6	7
S1	X					X	
S2		X			X		
S3			X				X
S4				X			X

(i) Determine the set of Forbidden Latencies and Permissible Latencies, and the Initial Collision Vector.
(ii) Draw the state diagram for scheduling this pipeline
(iii) List all simple cycles. Especially point out the Greedy Cycles (GC).
(iv) What is the Minimum Average Latency (MAL) of the pipeline? Specify lower and upper bounds of MAL? *[(CO5)(Apply/IOCQ)]*

(3 × 4) = 12

Group - E

8. (a) Draw the data flow diagram of the following instructions:
P = X + Y
Q = P / Y
R = X x P
S = R – Q
T = R x P
U = S / T. *[(CO6)(Apply/IOCQ)]*

(b) State the differences between control flow and data flow machine. *[(CO6)(Understand/LOCQ)]*

6 + 6 = 12

9. (a) Discuss Flynn's classification of processors. *[(CO6)(Remember/LOCQ)]*

(b) Draw the different components of the hardware control unit. *[(CO6)(Understand/LOCQ)]*

(c) Compare between the vector and array processors. *[(CO6)(Understand/LOCQ)]*

4 + 4 + 4 = 12

Cognition Level	*LOCQ*	*IOCQ*	*HOCQ*
Percentage distribution	*28.12*	*66.67*	*5.20*

Course Outcome (CO):

After the completion of the course students will be able to

1. Describe and explain the difference between computer organization and computer architecture.
2. Design the ALU for different arithmetical and logical problems and apply the knowledge of different multiplication and division algorithm.
3. Formulate design methodology for using various types of instructions.
4. Differentiate between different Memory hierarchy (Primary, Secondary, Cache). Able to solve different kind of numerical based on memory technologies and page replacement techniques.
5. Differentiate between types of pipeline, hazards and selecting remedial techniques to handle the hazards. able to distinguish between parallel architectures. Compare performance parameters of pipelines and deduce derivations to demonstrate change in performance parameters when branching is introduced. Able to solve numerical based on pipeline concepts.
6. Comparing techniques of ILP, types of CU, types of shared memory architectures. Distinguish between different multiprocessor architectures, Data Flow architecture, RISC and CISC architecture.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*