DIGITAL LOGIC (ECEN 2104)

Time Allotted: 2½ hrs Full Marks: 60

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

			Gro	up – A			
1.	Answe	er any twelve:			1	2 × 1 = 12	
		Choo	ose the correct alt	ernative for the f	ollowing		
	(i)	(i) The number system which use only 0-7 so (a) binary number (c) hexadecimal number			symbol is known as (b) octal number (d) all of these.		
	 (ii) The code used for labelling cells of the (a) Natural BCD (c) Gray (iii) The OR operation can be produced with (a) Two NOR gates (c) Four NAND gates 			(b) He	e K-map is (b) Hexadecimal (d) Octal.		
				(b) Th	with (b) Three NAND gates (d) Both answers (a) and (b)		
	(iv)	Simplified form (a) 1	of Boolean expre (b) 0	ession $(A + B' + A')$ (c) C	B) C is (d) C'		
	(v)	The minimum n (a) 3	number of 2-input (b) 4	NAND gates red (c) 5	quired to realize a hal (d) 6.	f-adder is	
	(vi)	Which of the fol (a) 1001	lowing is an inva (b) 0101	lid code combina (c) 1100	ation in 8421 BCD cod (d) 0111.	le?	
	(vii)	In which of the (a) Base 10	following base sy (b) Base 8	stems 123 is not (c) Base 2	a valid number? (d) Base 16.		
	(viii)	Digital circuit ca (a) AND	an be made by rep (b) NOT	peated use of wh (c) NOR	ich gates only? (d) OR.		
	(ix)	Select the type of logic circuit whose output depends not only on the preservalue of its input signals but also on the history of its inputs. (a) Combinational logic circuits (b) Sequential logic circuits (c) Both Combinational & Sequential logic circuits (d) None of these.				he present	

(x)	If $(212)_x = (23)_{10}$, then the value of (a) 2 (b) 3	x is (c) 4	(d) 5.			
		with the correct word				
(xi)	Binary equivalent of decimal num	nber 14 is				
(xii)	The invalid range for an input to TTL logic is from					
(xiii)	Octal equivalent of the binary number 010111101 is					
(xiv)	A logic circuit that can store one bit of information is a					
(xv)	In 2's complement representation of a negative number (using 8 bits) 1 0010101 in decimal is written as					
	Gro	oup - B				
(a) (b)	Simplify the Boolean expression X.Y+X(Y+Z)+Y(Y+Z). [(CO1)(Apply/IOCO) Convert the given function into canonical (SOP) form $f(A, B, C,D) = A.B + B.C'.D + A'.D$					
(c)	Simplify using K-map in SOP form. $f(A,B,C,D) = \Sigma (1,2,4,5,9,10) + \Sigma d$ (d=don't care).					
(a) (b) (c)	Implement two input Ex-OR gate Express the function $Y = A + \overline{B}C$ in Convert (78) ₁₀ to gray code.		[(CO1)(Analyse/HOCQ)] $[(CO1)(Apply/IOCQ)]$ $[(CO1)(Understand/LOCQ)]$ $5 + 5 + 2 = 12$			
	Gro	oup - C				
(a) (b) (c)	Design a 3 bit even parity gene checker circuit. Implement a full-adder circuit us Explain the operation of an octal	sing decoder and OR g	[(CO2)(Apply/IOCQ)]			
(a) (b)	Design 8:1 multiplexer using 4:1 Implement the logic function F (A	multiplexers. (0,1,3,4,8,5)	[(CO1)(Analyse/HOCQ)] 9,15) using 8:1 multiplexer.			
	Consider B, C, D as select lines.	ш	[(CO1)(Analyse/HOCQ)] 6 + 6 = 12			
	Gro	oup - D				
(2)	What are the difference between	asynchronous and sy	nchronous countars?			

2.

3.

4.

5.

6.

[(CO2)(Analyse/HOCQ)]

(b) What is race around condition or racing in JK flip-flop. Design Master-Slave JK flip-flop circuit to overcome this problem. [(CO2,CO3)(Apply/IOCQ)]

$$2 + (3 + 7) = 12$$

7. (a) Convert a S-R flip flop to D and T flip flop.

[(CO3)(Apply/IOCQ)]

(b) Design a synchronous counter using D flip flop that goes through the states 0-1-2-3-4-0. [(CO3)(Evaluate/HOCQ)]

$$(3+3)+6=12$$

Group - E

- 8. (a) Explain the working principle of SERIAL-IN, PARALLEL-OUT shift register with suitable logic diagram. [(CO2)(Apply/IOCQ)]
 - (b) What are ROM and RAM? What are the basic differences between EPROM and EEROM? [(CO4)(Remember/LOCQ)]
 - (c) What functions does a PLD programmer perform? What are the applications of PLA? [(CO4)(Apply/IOCQ)]

$$4 + (2 + 2) + (2 + 2) = 12$$

- 9. (a) Implement the function Y= (A+B)' using CMOS logic circuit. [(CO5)(Analyse/HOCQ)]
 - (b) Draw a NOR Gate using RTL logic circuit. [(CO5,CO6)(Remember/LOCQ)]
 - (c) Draw the circuit of TTL NAND gate.

[(CO5,CO6)(Remember/LOCQ)]

6 + 3 + 3 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	12.5	51.04	36.46

Course Outcome (CO):

After the completion of the course students will be able to

ECEN2104.1. Students will learn Binary Number system, and logic design using combinational gates.

ECEN2104.2. Students will design applications of Sequential Circuits.

ECEN2104.3. Students will design Finite State Machines.

ECEN2104.4. Students will learn Memory classifications.

ECEN2104.5.Students will learn basics of CMOS logic.

ECEN2104.6. Students will be prepared to learn various digital component design as used in VLSI Applications.

^{*}LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.