VLSI DESIGN, TESTING AND VERIFICATION
(VLSI 5202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The output of physical design is
(a) RTL (b) Veriog
(c) Layout (d) Circuit.

(ii) In Die Variation (IDV) means variation
(a) Within Wafer (b) Inside die
(c) Lot to Lot (d) Wafer to Wafer.

(iii) Data refresh operation is needed in
(a) SRAM (b) EROM
(c) EEPROM (d) DRAM.

(iv) Scan Design is needed to test
(a) Sequential Circuit (b) Combinational Circuit
(c) Stuck at Faults (d) All of (a), (b) & (c).

(v) VHDL is a
(a) Multi-threaded program (b) C like programming language
(c) Single user program (d) Sequential program.

(vi) Minimum Number of Transistors in TG XNOR gate is
(a) 2 (b) 4
(c) 6 (d) 12.

(vii) Smallest size Memory cell is
(a) Flip-Flop (b) SRAM
(c) Register File (d) DRAM.

(viii) Logic Synthesis translates descriptions from
(a) Physical to Behavioural (b) Structural to Physical
(c) Behavioural to Structural (d) Structural to Behavioural.

(ix) FPGA is a
(a) SOC (b) Semi custom ASIC
(c) Programmable ASIC (d) Full custom ASIC

(x) The critical path for a design refers to
(a) The path with no delay (b) The path with minimum delay
(c) The path with optimum delay (d) The path having maximum delay.

Group - B

2. (a) Explain briefly under what PVT condition, NMOS Transistor behaves slowest and why. *[(CO5)(Analyze/IOCQ)]*
(b) Explain how H-Tree Clock Network helps to reduce clock skew. *[(CO5)(Analyze/IOCQ)]*
6 + 6 = 12

3. (a) Explain write '0' followed by read '0' operation in 1-Transistor DRAM Circuit using circuit diagram and timing waveforms. *[(CO1)(Analyze/IOCQ)]*
(b) Explain sizing criteria of 6 Transistor SRAM cell. *[(CO1)(Analyze/IOCQ)]*
6 + 6 = 12

Group - C

4. (a) Sketch the Y chart for simplified VLSI design flow in three domains. *[(CO3)(Remember/LOCQ)]*
(b) How does STA (Static Timing Analysis) work? *[(CO3)(Analyze/IOCQ)]*
6 + 6 = 12

5. (a) Briefly explain components of interconnect capacitance. *[(CO2)(Understand/LOCQ)]*
(b) Why do driver side of a wire need to be of low resistance and receiver side of the wire need to be of low capacitance? Explain using Elmore Delay model. *[(CO2)(Analyze/IOCQ)]*
6 + 6 = 12

Group - D

6. (a) For a flip flop based sequential circuit, Cycle Time = 400ps, Setup Time = 50ps, Clock-Skew = 40ps, Combinational Delay = 260ps, Clock to Out Delay of Flop = 80ps. Hold Time = 80ps. What is setup margin and hold margin for the circuit? *[(CO4)(Evaluate/HOCQ)]*
(b) What is clock skew and what are the sources of clock skew? *[(CO5)(Remember/LOCQ)]*
6 + 6 = 12

7. (a) Design a two input XNOR gate using CMOS transmission gate switches. *[(CO3)(Evaluate/HOCQ)]*

   (b) Design a Transmission Gate implementation of the Level 1 D latch circuit. *[(CO3)(Evaluate/HOCQ)]*

6 + 6 = 12

Group - E

8. (a) What is input test pattern to detect Stuck-at-1 fault at the Output of a 2 input NOR gate? *[(CO6)(Evaluate/HOCQ)]*

   (b) Explain D-Algorithm using an example. *[(CO6)(Analyze/IOCQ)]*

6 + 6 = 12

9. (a) Explain how Level Sensitive Scan Design Flip Flop (LSSD-SFF) works using Circuit diagram. *[(CO6)(Analyze/IOCQ)]*

   (b) Generate primary input test patterns (i) for S-a-0 fault at output of 3 input NOR Gate and (ii) for S-a-1 fault at output of 3 input NAND Gate. *[(CO6)(Evaluate/HOCQ)]*

6 + (3 + 3) = 12

Cognition Level	*LOCQ*	*IOCQ*	*HOCQ*
Percentage distribution	*18.75*	*50*	*31.25*

Course Outcome (CO):

After the completion of the course students will be able to

1. Students will learn embedded Memory Design in VLSI Chip
2. Students will learn VLSI Interconnect Design
3. Students will learn Industry Standard STA (Static Timing Analysis) Method
4. Students will learn Set-up and hold Checks for Timing Verification
5. Students will learn process variation and Clock skew concepts
6. Students will learn Si Testing/Debug Methods

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*