LOW POWER VLSI DESIGN
(VLSI 5232)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The most dominant component of dynamic power dissipation in CMOS circuits is
(a) short circuit power dissipation (b) glitch power dissipation
(c) subthreshold leakage (d) switching power dissipation.

(ii) Short circuit power dissipation depends on
(a) frequency of the input signal (b)supply voltage
(c) rise/fall times of input signal (d) all of the above.

(iii) If rise time of input of an inverter is increased, then short circuit current
(a) increases linearly (b) decreases linearly
(c) remains same (d) decreases exponentially.

(iv) Short circuit power increases with
(a) increase in rise and fall times of input signal
(b) increase in the load capacitance
(c) decrease in the load capacitance
(d) both (a) and (c).

(v) Switching activity of a complex logic gate depends on
(a) the topology of the gate
(b) the statistical timing behaviour of the circuit
(c) both (a) and (b)
(d) none of the above

(vi) If the fan-in is more, the switching power dissipation of a gate
(a) would be more (b) would be less
(c) would remain invariant (d) would increase indefinitely.

(vii) SVS stands for
(a) Static Voltage Scaling (b) Small Voltage Scaling
(c) Sequential Voltage Scaling (d) Staggered Voltage Scaling.

(viii) Parallel processing may be used for
(a) higher performance
(b) lower power consumption
(c) higher performance and lower power consumption
(d) lower performance and higher power consumption.

(ix) High V_{dd} gates are usually associated with a
(a) high delay (b) low delay
(c) zero delay (d) infinite delay.

(x) Both power and delay reduction for a digital gate is possible if
(a) V_{dd} decreases (b) C_L decreases
(c) switching activity decreases (d) never possible.

Group - B

2. (a) Differentiate between dynamic and static power dissipation in CMOS circuits. Classify the different types of power dissipation in these circuits. *[(CO1)(Understand/LOCQ)]*
(b) What is switching activity in CMOS gates? *[(CO2)(Understand/LOCQ)]*
(c) Calculate the probability of transition of a NAND Gate considering equiprobable inputs. *[(CO2)(Evaluate/HOCQ)]*

5 + 2 + 5 = 12

3. (a) Derive an expression to show the dependence of short circuit power on the supply voltage, delay and speed of operation in CMOS circuits. *[(CO4)(Create/HOCQ)]*
(b) How does this power vary with the load capacitance? *[(CO4)(Apply/IOCQ)]*

10 + 2 = 12

Group - C

4. (a) How can the leakage currents in a MOSFET be classified? Illustrate with a suitable diagram. *[(CO3)(Apply/IOCQ)]*
(b) Explain the BTBT mechanism in a scaled MOSFET. *[(CO3)(Understand/LOCQ)]*

8 + 4 = 12

5. (a) Define the subthreshold slope. Show that the ideal value of the subthreshold slope is 60mV/decade. *[(CO3)(Apply/IOCQ)]*
(b) Why is a steep subthrehold slope desirable in low power VLSI circuits? *[(CO3)(Analyze/IOCQ)]*
(c) Analyze the dependence of the Subthreshold slope on the substrate bias applied to a MOSFET. *[(CO3)(Analyze/IOCQ)]*

6 + 2 + 4 = 12

Group - D

6. (a) Illustrate with a suitable example the occurrence of glitch power. *[(CO3)(Understand/LOCQ)]*
   (b) How can it be minimized? *[(CO2)(Apply/IOCQ)]*
   (c) What are the various components of Load Capacitance (C_L) in digital circuits? *[(CO1)(Remember/LOCQ)]*

5 + 1 + 6 = 12

7. (a) What is standby leakage power dissipation? *[(CO3)(Remember/LOCQ)]*
   (b) Explain how standby leakage power may be reduced in MTCMOS technique. *[(CO3)(Understand/LOCQ)]*
   (c) Discuss its advantages and disadvantages. *[(CO3)(Analyze/IOCQ)]*

1 + 9 + 2 = 12

Group - E

8. (a) State the basic idea of the pipelining approach of architecture design for low power circuits. *[(CO6)(Understand/LOCQ)]*
   (b) Prove that the power dissipation is 0.28 times that of a typical reference architecture using the pipelining approach. *[(CO6)(Evaluate/HOCQ)]*
   (c) Point out the advantages offered by the pipelining technique. *[(CO6)(Analyse/IOCQ)]*

2 + 8 + 2 = 12

9. (a) Discuss how low power can be achieved in multi-core processors. *[(CO6)(Apply/IOCQ)]*
   (b) Show how you can combine pipelining and parallelism to achieve low power instead of higher performance? *[(CO6)(Analyse/IOCQ)]*

6 + 6 = 12

Cognition Level	*LOCQ*	*IOCQ*	*HOCQ*
Percentage distribution	*35.42*	*40.62*	*23.96*

Course Outcome (CO):

After the completion of the course students will be able to

1. Students will learn source of CMOS Dynamic Power Dissipation
2. Students will learn CMOS Dynamic Power Reduction Techniques
3. Students will learn source of CMOS Standby (leakage) Power Dissipation & Reduction Techniques
4. Students will learn Short Circuit Power Reduction Techniques
5. Students will learn Embedded Memory Power Reduction Techniques
6. Students will learn System and Architecture level Power Reduction Techniques

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*