ANALOG VLSI IC DESIGN
(VLSI 5201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Ideal MOSFET can be considered as a constant current source when operated in
(a) Triode region (b) Deep triode region
(c) saturation region (d) None of the above.

(ii) Practical current mirror circuits deviate from the ideal behaviour due to
(a) Channel length modulation effect (b) Threshold voltage offset between two transistors
(c) Imperfect geometrical matching (d) All of the above.

(iii) A digital-to-analog converter is considered to be non-monotonic if it exhibits
(a) *+ DNL* (b) *– DNL*
(c) *+ INL* (d) *– INL.*
where, the notations have their usual significance.

(iv) *RMS* quantization noise of a *ADC* can be given by (if the quantization level is '*q*')
(a) *q/12* (b) $q^{1/2}$
(c) $q^{-1/2}$ (d) *q/2.*

(v) For push-pull amplifier operation
(a) NMOS will be in saturation, PMOS will be in linear mode
(b) NMOS will be in linear, PMOS will be in saturation mode
(c) Both NMOS and PMOS will be in saturation mode
(d) Both NMOS and PMOS will be in linear mode.

(vi) The frequency of the signal applied to the switched-capacitor circuit should satisfy the criteria
(a) $f_{signal} << f_{clock}$ (b) $f_{signal} >> f_{clock}$
(c) $f_{signal} = 2f_{clock}$ (d) $f_{clock} = 2f_{signal}$

(vii) If the substrate terminals of the transistors forming the source-coupled pair of the *CMOS* differential amplifier is connected to ground, then,
(a) threshold voltages depend on C_{bd} and C_{bs} (b) threshold voltages decrease nonlinearly
(c) threshold voltages decrease linearly (d) threshold voltages increase.

(viii) A differential signal is defined as the one that is measured between
(a) a node and the ground
(b) two nodes having equal & opposite signal excursions around a fixed potential & also exhibiting equal impedances to that potential
(c) two nodes having equal & opposite signal excursions around a fixed potential & but exhibiting unequal impedances to that potential
(d) two nodes having equal & identical signal excursions around a fixed potential & also exhibiting equal impedances to that potential.

(ix) An ideal differential amplifier should have *CMRR*
(a) $0 < CMRR < 1$ (b) One (c) Infinite (d) Zero.

(x) A *4-bit R/2R* digital-to-analog converter has a reference of *5volts*. What is the analog output for the input code *0101*
(a) 0.3125 V (b) 3.125 V (c) 0.78125 V (d) -3.125 V.

Group- B

2. (a) Explain the key principle of operation of an enhancement-type *MOSFET*. *[(CO1)(Understand/LOCQ)]*
(b) Can a MOSFET be modelled as an ideal switch? Justify. *[(CO1)(Apply/IOCQ)]*
(c) It is required to design the circuit of *Fig.1* to establish a dc drain current $I_D = 0.5\ mA$. The *MOSFET* is specified to have $V_{th} = 1\ V$ and $k_n'(W/L) = 1\ mA/V^2$. For simplicity, neglect the channel length modulation effect. Use a power – supply $V_{DD} = 15\ V$.

Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n'(W/L)$ but $V_{th} = 1.5\ V$.

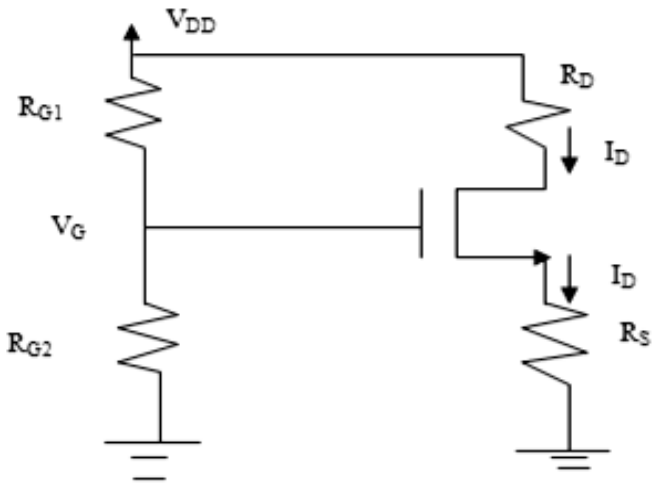

Fig. 1

[(CO1)(Create/HOCQ)]

3 + 5 + 4 = 12

3. (a) Explain the principle used to increase the small-signal output resistance of a current sink with proper circuit diagram.
[(CO1)(Understand /LOCQ)]

(b) Derive the small-signal voltage gain of an active *PMOS* load inverting amplifier from its small-signal equivalent circuit.
[(CO2)(Analyze/IOCQ)]

(c) For a MOS differential pair with a common-mode voltage V_{CM} applied as shown in *Fig.2*, let $V_{DD} = V_{SS} = 1.5\ V$, $k_n'(W/L) = 4\ mA/V^2$, $V_{th} = 0.5\ V$, $I = 0.4\ mA$, $R_D = 2.5\ k\Omega$. Neglect the channel-length modulation effect. Calculate V_{OV} *and* V_{GS} for each transistor. For $V_{CM} = 0$, find V_S, i_{D1}, i_{D2}, V_{D1}, *and* V_{D2}. Evaluate the highest value of V_{CM} for which both *Q1* and *Q2* remain in saturation.
[(CO2)(Evaluate/HOCQ)]

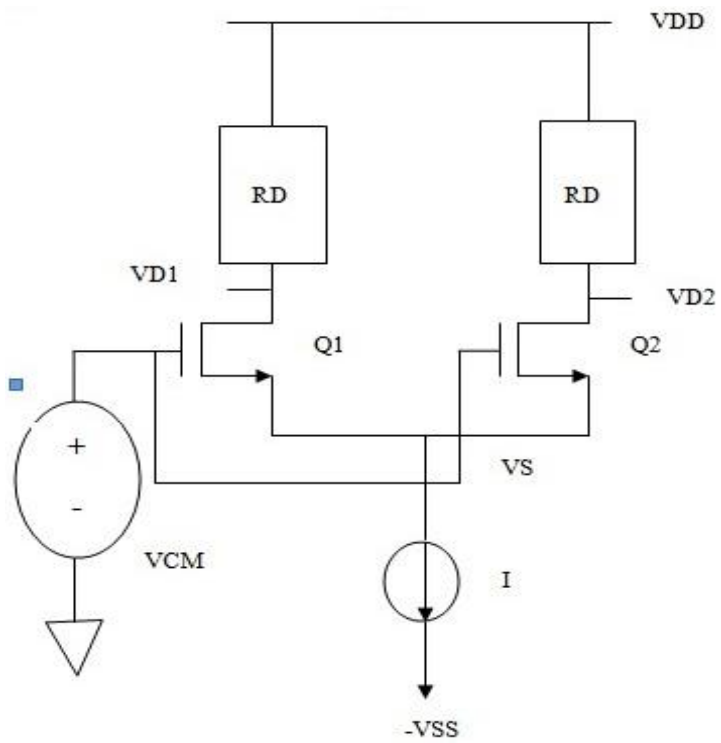

Fig. 2

4 + 5 + 3 = 12

Group - C

4. (a) Mention the features of a well designed transformer. *[(CO3)(Understand/LOCQ)]*

(b) Does "Current Crowding" effect influence inductance and capacitance of spiral geometry of inductors? Justify your answer. *[(CO3)(Analyze/IOCQ)]*

(c) Analyze if the following in Fig.3 can be considered for small coupling mentioning the pros and cons of this topology.
[(CO3)(Analyze /IOCQ)]

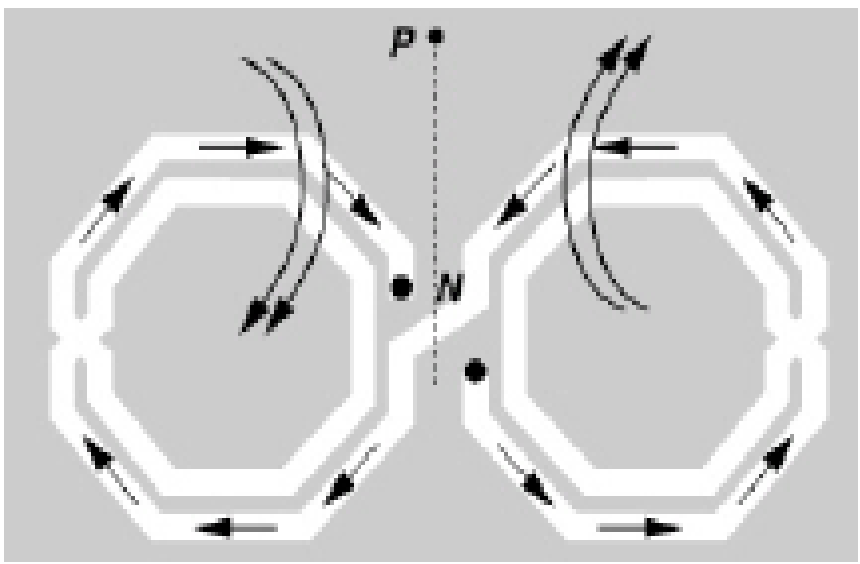

Fig. 3

4 + 5 + 3 = 12

5. (a) Mention the key issues to be taken into account for modelling of spiral inductor. *[(CO3)(Understand/LOCQ)]*
   (b) Analyze the parasitic capacitances of the spiral inductors using suitable equivalent model for this network. *[(CO3)(Analyze/IOCQ)]*
   (c) An engineer wishes to design a spiral inductor for a 900 MHz GSM system. Determine if the *5 nH* structure suited for this application. *[(CO3)(Evaluate/HOCQ)]*

4 + 5 + 3 = 12

Group - D

6. (a) Explain the operation of sample-and-hold circuit in analog-to-digital converters. *[(CO4)(Understand/LOCQ)]*
   (b) Find the maximum sampling error for a *S/H* circuit that is sampling a sinusoidal input signal that could be described as $V_{in} = A\ Sin2\pi ft$, where, *A* is *2 V* and $f = 100\ kHz$. Assume that the aperture uncertainty is equal to *0.5 nS*. *[(CO4)(Apply/IOCQ)]*
   (c) Evaluate the maximum resolution of an *ADC* which can use the above *S/H* circuit while maintaining a sampling error less than *0.5 LSBs*. *[(CO4)(Evaluate/HOCQ)]*

4 + 5 + 3 = 12

7. (a) Explain *INL* and *DNL* of a digital-to-analog converter graphically. *[(CO4)(Understand/LOCQ)]*
   (b) Determine the *DNL* for the *3*-bit nonideal *DAC* whose transfer curve is shown in Fig. 4. Assume that, $V_{REF} = 5\ V$. *[(CO4)(Apply/IOCQ)]*

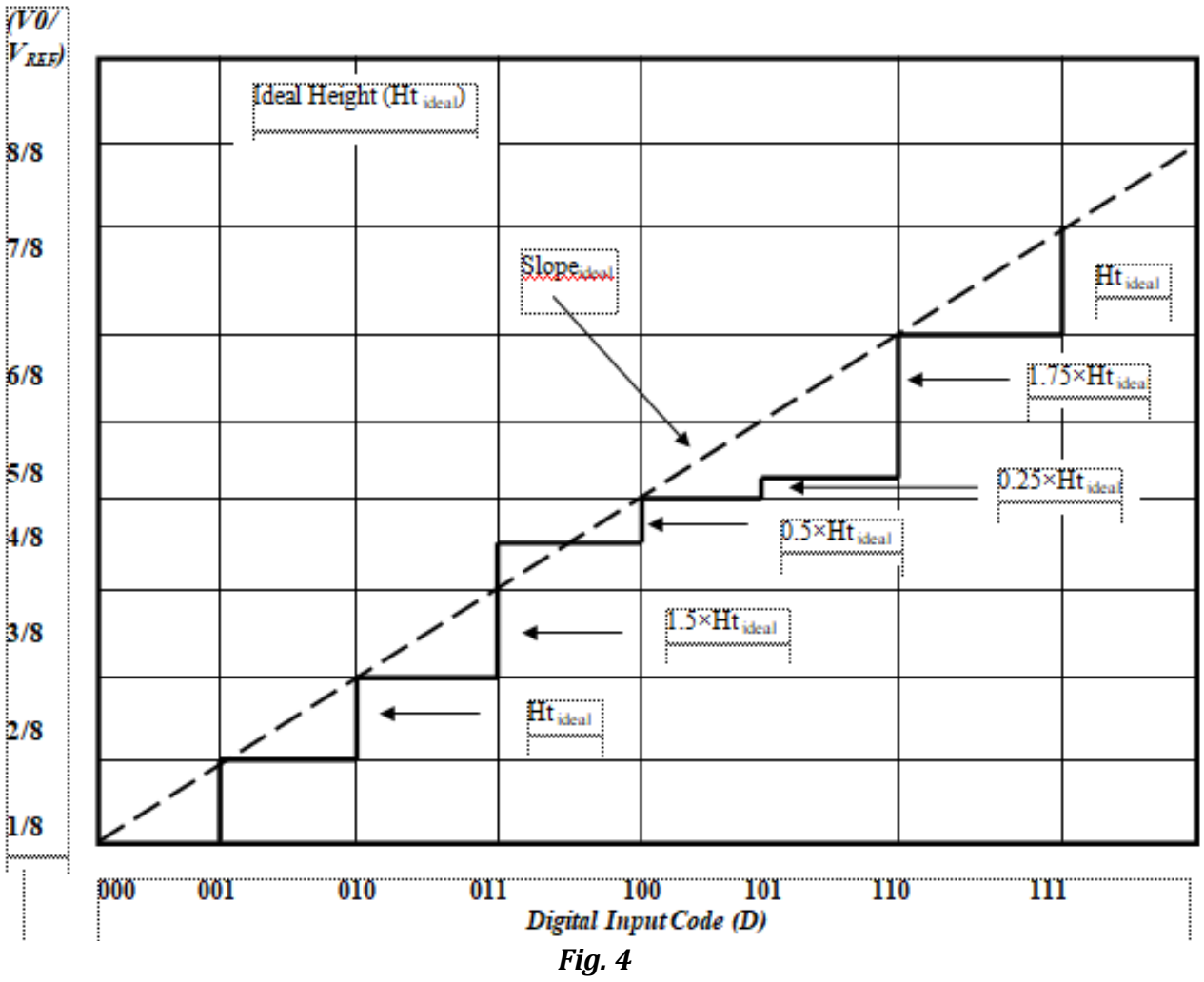

Fig. 4

(c) Plot the *DNL* curve evaluated for the non-ideal *3-bit DAC*. *[(CO4)(Evaluate/HOCQ)]*

4 + 5 + 3 = 12

Group - E

8. (a) Mention the disadvantages of the switched-capacitor circuits. *[(CO5)(Remember/LOCQ)]*
   (b) The accuracy is the primary reason for wide spread use of switched-capacitor circuits in *CMOS* technology – Justify the statement. *[(CO5)(Apply/IOCQ)]*
   (c) Calculate the minimum and maximum on-resistance of *M1* in Fig. 5. Assume, $\mu_n C_{OX} = 50\mu A/V^2$, $(W/L) = (10/1)$, $V_{th} = 0.7V$, $V_{DD} = 3V$ *and* $\gamma = 0$. *[(CO5)(Evaluate/HOCQ)]*

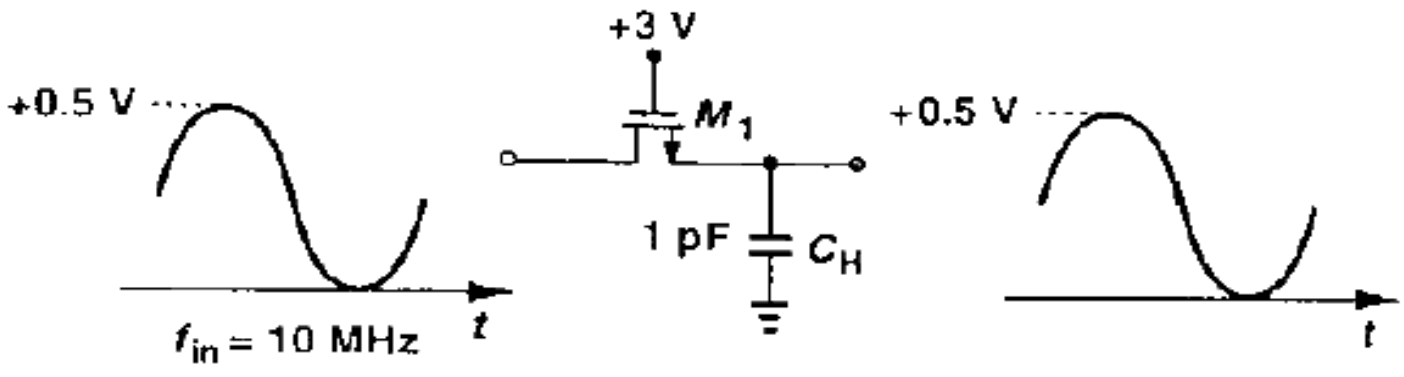

Fig.5

4 + 5 + 3 = 12

9. (a) Explain the Barkhausen criteria for oscillation. *[(CO6)(Understand/LOCQ)]*

(b) Derive the formula for the oscillation period (T_{osc}) of the voltage-controlled oscillator. *[(CO6)(Analyze/IOCQ)]*

(c) Design a bistable circuit using ring of inverters and evaluate the number of stages (n) required for that? *[(CO6)(Evaluate/HOCQ)]*

4 + 5 + 3 = 12

Cognition Level	*LOCQ*	*IOCQ*	*HOCQ*
Percentage distribution	*32.30*	*44.80*	*22.90*

Course Outcome (CO):

After the completion of the course students will be able to

1. Understand and analyze MOS-based analog VLSI sub-circuits, relevant small-signal equivalent circuit models and design them *eg.* current mirrors.
2. Design and analyze MOS circuits of practical importance eg. common-source amplifiers and differential amplifiers
3. Understand the basic concepts in RF design and the geometry, models of passive devices used in RFIC.
4. Understand the principle of operation, characterization of the data converter circuits and design them.
5. Understand and analyze the different topologies of switched-capacitor circuits and apply the concept for the analysis of circuits of practical applications.
6. Understand the principle of operation of the oscillator circuit and apply the concept for the analysis of circuits of practical applications.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*