ADVANCED VLSI PROCESSOR
(VLSI 5241)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) A computer process is a macro as it applies to an initial state and generates a
(a) Program (b) Data
(c) Undefined State (d) Final State.

(ii) Basic computer instruction cycle consists of
(a) read, write, storage (b) fetch, decode, execute
(c) decode, fetch, store (d) read, fetch, store.

(iii) Computers with R/M architecture have Instructions which can operate both on registers with one of the operands in
(a) register (b) temporary variable
(c) memory (d) board.

(iv) TMS320C6X DSPs supports _____ architecture so they have a number of processing units and data paths.
(a) Von Neumann (b) Harvard
(c) VLIW (d) IBM

(v) ALU is an integral part of
(a) CU (b) CPU
(c) Memory unit (d) I/O unit.

(vi) Vector processor belongs to the Flynns taxonomy class of _____ processors.
(a) MISD (b) SISD
(c) SIMD (d) MIMD

(vii) ARM based processor is a _____ processor.
(a) CISC (b) RISC
(c) VLIW (d) DSP

(viii) Microinstructions consists of _____ and are stored in the _____ _____.
(a) micro-operations, control, memory (b) fake-operations, cache, memory
(c) micro-operations, cache, memory (d) micro-operations, flash, memory

(ix) Thumb instruction set belongs to which architecture family?
(a) Intel Polaris (b) DSP chip TMS320C5X
(c) ARM (d) DSP5600X from MOTOROLA.

(x) In parallel computing, granularity means the amount of computation in relation to _____
(a) communication (b) cpu
(c) controller (d) memory.

Group–B

2. (a) Distinguish between computer architecture and organization. Compare Harvard, Von Neumann and Modified Harvard Architecture and illustrate these architecture using block diagram. *[(CO4) (Remember/LOCQ)]*

(b) Given a 128 × 8 ROM chip with an enable input, show the external connections necessary to build a 512 × 16 ROM using 8 chips and decoder. *[(CO2) (Understand/LOCQ)]*

(c) Evaluate X = (A + B*E + C)/D; using zero address, and one address instruction machine. *[(CO1) (Analyze/IOCQ)]*

(1 + 3) + 4 + (2 + 2) = 12

3. (a) The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A two word call subroutine is located in memory at address 1120 followed by the address field of 6720 at location at location 1121. What are the contents of PC, SP and the top of stack?
(i) before the call instruction is fetched.
(ii) after the call instruction is executed, and
(iii) after the return from subroutine? *[(CO1) (Evaluate/HOCQ)]*

(b) Compare between properties of RISC and CISC architecture, and mention the plus points of each system. *[(CO2) (Remember/LOCQ)]*

6 + 6 = 12

Group – C

4. (a) Find the RAW, WAR and WAW and potential control hazards in the following code

```
        LOAD R1 ← M[312]
        ADD R2 ← R2 + R1
        JC LABEL1
        ADD R3 ← R3 + 1
        STORE R2 ← R1 + R3
LABEL1: STORE R1 ← R2+ R3
```

[(CO2) (Analyze/IOCQ)]

(b) A non pipeline takes 40 ns to complete a task. The same task can be processed in 4 segment pipeline with a clock cycle of 4 ns. Determine the speed up ratio of the pipe line for 50 tasks. What is the maximum speed up that can be achieved in this case? *[(CO2) (Evaluate/HOCQ)]*

6 + 6 = 12

5. (a) How does DRAM help with speed up? *[(CO1) (Analyze/IOCQ)]*
   (b) Briefly describe the on chip peripheral units in TMS320C5X. *[(CO3) (Remember/LOCQ)]*
   (c) Initially let the content of data memory location 1500h be 678 Ah, and content of register R0 be C234h. Describe the content of the register R0 and memory location 1500h after execution of instruction
   (i) LMMR AR0, #1500
   (ii) SMMR AR0, #1500. *[(CO3)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

Group - D

6. (a) Describe hardware accelerator with proper example and mention its uses. *[(CO4)(Remember/LOCQ)]*
   (b) Discuss the types of parallelism used by accelerator to achieve faster computing speed. Which are the parameters to be considered for an accelerator design? *[(CO4) (Analyze/IOCQ)]*

6 + 6 = 12

7. (a) For ARM7 briefly describe the various operating modes and the register organization for general and privileged modes. *[(CO5) (Understand/LOCQ)]*
   (b) For the ARM instruction set illustrate load, store, arithmetic and logical instructions with and without condition codes. *[(CO5) (Apply/IOCQ)]*

6 + 6 = 12

Group - E

8. (a) What is fine and coarse grained granularity in terms of parallel programming and data usage? *[(CO5) (Remember/LOCQ)]*
   (b) What are limitations of uniprocessor? How does a CMP (Chip Multi Processor) resolve those issues? *[(CO5) (Understand/LOCQ)]*
   (c) What is a SOC and what are its application? *[(CO6) (Remember/IOCQ)]*

2 + (2 + 4) + 4 = 12

9. (a) Classify the Uni and Multi processors following Flynns Taxonomy. *[(CO5) (Remember/LOCQ)]*
   (b) What is UMA and NUMA? What are their relative pros and cons? *[(CO5) (Understand/LOCQ)]*
   (c) What is a Multithreaded processor? Explain its different types. *[(CO5) (Understand/IOCQ)]*

4 + 4 + 4 = 12

Cognition Level	*LOCQ*	*IOCQ*	*HOCQ*
Percentage distribution	*47.92*	*35.42*	*16.66*

Course Outcome (CO):

After the completion of the course students will be able to
1. Students will learn basic structure of instruction set architecture (ISA)
2. Students will learn CISC and RISC Architecture
3. Students will learn sample DSP Processor Architecture
4. Students will learn Accelerator
5. Students will learn Multi-Threaded Processor
6. Students will learn use of Microprocessor cores in SOC Design

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*