ADVANCED NANO DEVICES
(VLSI 5242)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The principle of the MOSFET operation is
(a) control the conduction of current between the source and the drain, using the potential difference applied at the gate voltage as a control variable
(b) control the current conduction between the source and the gate, using the electric field applied at the drain voltage as a control variable
(c) control the current conduction between the PN junction, using the electric field generated by the bias voltage as a control variable
(d) control the current conduction between the PN junctions, using the electric potential generated by the gate voltage as a control variable.

(ii) Consider the following statements for a metal oxide semiconductor field effect transistor (MOSFET):
P: As channel length reduces, OFF – state current increases.
Q: As channel length reduces, output resistance increases.
R: As channel length reduces, threshold voltage remains constant.
S: As channel reduces, ON current increases.
Which of the above statements are INCORRECT?
(a) P and Q (b) P and S (c) Q and R (d) R and S.

(iii) The depletion region of PN junction is one, that is depleted of
(a) atoms (b) mobile charges
(c) immobile charges (d) velocity of the carriers.

(iv) The effective channel length of a MOSFET in saturation decreases with increase in
(a) Gate voltage (b) Drain voltage
(c) Source voltage (d) Body voltage.

(v) For an n–channel enhancement type MOSFET, if the source is connected at a higher potential than that of the bulk (i.e. VSB > 0), the threshold voltage V_T of the MOSFET will
(a) remain unchanged (b) decrease
(c) change polarity (d) increase.

(vi) In a MOSFET operating in the saturation region, the channel length modulation effect causes
(a) an increase in the gate – source capacitance
(b) a decrease in the transconductance
(c) a decrease in the unity – gain cut – off frequency
(d) a decrease in the output resistance.

(vii) The cut off frequency, f_T of the MOSFET is
(a) proportional to transconductance(g_m) and inversely proportional to total capacitance between gate to source/drain (Cgs+ Cgd)
(b) proportional to transconductance(g_m) and total capacitance between gate to source/drain (Cgs+ Cgd)
(c) inversely proportional to transconductance(g_m) and total capacitance between gate to source/drain (Cgs+ Cgd)
(d) inversely proportional to transconductance(g_m) and total capacitance between gate to source/drain (Cgs+ Cgd).

(viii) The depletion mode n-MOS differs from enhancement mode n-MOS in
(a) threshold voltage (b) channel Length.
(c) switching time (d) none of the mentioned.

(ix) Velocity saturation in a short channel device causes the drain current to saturate at
(a) same V_{ds} (b) lower V_{ds} (c) higher V_{ds} (d) V_t

(x) The conduction of current I_D depends on
(i) Gate to source voltage (ii) Drain to source voltage
(iii) Bulk to source voltage (iv) Threshold voltage
(v) Dimensions of MOSFET
(a) Only i (b) Only i, ii and iii
(c) Only v (d) All of the mentioned.

Group – B

2. (a) Explain why supply voltage scaling makes the device slower. *[CO1/Create/HOCQ]*
(b) Derive the relationship between subthreshold swing and gate oxide capacitance. Why subthreshold swing is always higher than 60db/decade for a conventional MOSFET device. *[CO1/Evaluate/HOCQ]*

4 + (4 + 4) = 12

3. (a) Explain channel length modulation and its effects on drain current? Describe body effect in MOSFET. *[CO1/Analyse/IOCQ]*
(b) To determine the inversion carrier mobility from experimental results, consider an n channel MOSFET having channel width 15 μm, channel length 2 μm and Cox = 6.9×10^{-8} F/cm^2. Assume that the drain current in the non saturation region for V_{DS} = 0.1 V is I_D =35 μA at V_{GS} = 1.5 V and I_D = 75 μA at V_{GS} = 2.5 V. *[CO1/ Evaluate /IOCQ]*

(3 + 3) + 6 = 12

Group – C

4. (a) How does a work function difference cause band bending in equilibrium in Metal-Oxide-Semiconductor (MOS)? *[CO1/Analyse/IOCQ]*

   (b) Differentiate between Partially-Depleted (PD) and Fully-Depleted (FD) Silicon-on-Insulator MOSFETs. *[CO3/Analyse/IOCQ]*

6 + 6 = 12

5. (a) Justify the use of high K-dielectric material in MOSFET. Explain the concept of Equivalent Oxide Thickness. *[CO2/Understand/LOCQ]*

   (b) How high K plus metal gate transistor reduces gate leakage significantly compared to traditional silicon dioxide insulator plus poly gate transistor? *[CO2/ Understand /LOCQ]*

(4 + 4) + 4 = 12

Group - D

6. (a) What is parasitic capacitance? What are sources of parasitic capacitances in the MOSFET? *[CO1/Understand/LOCQ]*

   (b) Draw the small signal equivalent circuit of a MOSFET and show the parasitic capacitances in it. *[CO1/Create/HOCQ]*

(2 + 4) + 6 = 12

7. (a) Explain why FinFETs have better immunity to the Short Channel Effects? *[CO4/Analyse/IOCQ]*

   (b) Describe with the help of necessary illustration why ON resistance increases in the Double Gate underlap MOSFET structure. *[CO4/Analyse/IOCQ]*

   (c) Explain how ON current (Ion) is improved and DIBL is suppressed in the Double Gate Underlap MOSFET structure. *[CO4/Analyse/IOCQ]*

4 + 4 + 4 = 12

Group – E

8. (a) Explain the advantages and disadvantages of underlap MOSFET structure. *[CO4/Remember/LOCQ]*

   (b) Is the overlap of the gate with the source and drain regions required, beneficial or irrelevant? *[CO4/Understand/LOCQ]*

   (c) How to improve the ON current in the underlap MOSFET structure? *[CO4/Understand/LOCQ]*

4 + 4 + 4 = 12

9. (a) How substrate doping influences SCE? Explain how Multiple Threshold Voltage devices can reduce leakage power significantly without compromising chip frequency. *[CO3/Analyse/LOCQ]*

   (b) Draw the cross-sectional diagram of DG MOS HEMT and explain the operation of a DG MOS HEMT with the help of necessary illustration. *[CO4/Analyse/IOCQ]*

(2 + 3) + (3 + 4) = 12

Cognition Level	*LOCQ*	*IOCQ*	*HOCQ*
Percentage distribution	*36.46*	*44.79*	*18.75*

Course Outcome (CO):

1. Students will learn various leakage phenomena in advanced MOS.
2. Students will learn High K Plus Metal Gate Technology for advanced Process Nodes.
3. Students will learn SOI MOS device.
4. Students will learn FinFET Devices like DGMOS, Tri-gate.
5. Students will learn Hetero-Structures.
6. Students will learn CNT, Graphene Device.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*