REAL TIME EMBEDDED SYSTEM
(ECEN 4241)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) For embedded systems, the RTOS resides in
(a) RAM (b) EPROM (c) Flash Memory (d) None of (a), (b) & (c).

(ii) In the sleep mode,
(a) the clock is stopped (b) the buses are in z-state
(c) the address bus is in z-state (d) the data bus is in z-state.

(iii) I^2C is a
(a) Parallel bus protocol (b) Serial bus protocol
(c) Two wire protocol (d) Both (b) & (c) are true.

(iv) For a multiplexed 7-segment display consisting of 4 display units, number of signals (for display and control together), will be (don't consider multiplexer)
(a) 32 (b) 30 (c) 10 (d) 11.

(v) Watchdog timers help multiple tries for a password automatically. The number of tries is
(a) 3 (b) 4 (c) 5 (d) Decided by the administrator

(vi) A 64-key key-board in a microprocessor system requires for its interfacing row-lines and column-lines. Total number of lines is
(a) 18 (b) 14 (c) 16 (d) none of (a), (b) & (c).

(vii) Number of Transistors used in DRAM cell is _____.
(a) 3 (b) 2 (c) 4 (d) 5

(viii) In USB 2.0 transmission the bus lines 'data+' and 'data-' has a phase difference of magnitude _____.
(a) 0 deg (b) 90 deg (c) 180 deg (d) 360 deg

(ix) Property which is not useful for RTOS is
(a) Deterministic (b) Time Sensitive
(c) Low interrupt latency (d) Can use Virtual Memory.

(x) The ARM processors memory access instructions are usually limited to
(a) LOAD instructions only (b) all instructions like 8086
(c) STORE instructions only (d) LOAD and STORE instructions.

Group - B

2. (a) There are some common design metrics for an ideal embedded system. Discuss briefly about six of them. What are the main differences between ASIC and FPGA? Why is FPGA preferred in circuits? [(CO1)(Remember/LOCQ)]
(b) Why is time-to-market critical for a new product? Explain. [(CO1)(Understand/IOCQ)]
(6 + 3) + 3 = 12

3. (a) Differentiate between a CISC and a RISC computer. Give examples of both types. [(CO2)(Remember/LOCQ)]
(b) Explain what is Von Neumann bottleneck. [(CO2)(Understand/IOCQ)]
(c) In embedded systems, microcontrollers are used which supports three modes of operation-active, stand-by and sleep. Elucidate the differences between the 3 modes and justify the importance of the Sleep mode in power saving applications. [(CO3)(Understand/LOCQ)]
4 + 3 + 5 = 12

Group - C

4. (a) A Bus is like a street and a Port is like a driveway- establish the analogy. Show with block diagrams the two protocols of data transfer between a Master and a Slave:
(i) strobe aided and (ii) via handshake. Draw the timing diagrams for both. [(CO3)(Analyse/IOCQ)]
(b) I^2C is a serial protocol developed by Philips semiconductors for serial communication. It uses only two lines – SCL and SDA. Show with timing diagrams the following events:
(i) Start; (ii) Sending '0' bit; (iii) Sending '1' bit and (iv) Stop condition. [(CO2)(Analyze/HOCQ)]
(2 + 4) + 6 = 12

5. (a) Operation "fetch" is a part of what cycle? What are other components of that cycle? Control memory is used in which type of Control unit design and how? What are micro-instruction and micro-operation? If speed is priority then which control unit design is preferred and why? [(CO2)(Understand/LOCQ)]
(b) A clocked sequential circuit with output A and inputs X and Y uses a D flip flop. The next-state values are obtained from the state equation as : A(t+1) = A(t) xor X(t) xor Y(t). Show the State table, State diagram, Excitation table, and the circuit diagram. [(CO3)(Analyze/IOCQ)]
(1 + 1 + 1 + 2 + 1) + 6 = 12

Group - D

6. (a) A DMA controller transfers 16 bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at 2400 bauds. The CPU is fetching and executing instructions at an average rate of 1 million instructions per sec. By how much will the CPU be slowed down because of the DMA transfer. [(CO4)(Apply/HOCQ)]

   (b) Outline the basic principles of memory management technique with virtual memory, page table and page size? What is demand paging, page fault, page and page replacement policies? [(CO3)(Remember/LOCQ)]

4 + [3 + (2 + 3)] = 12

7. (a) Distinguish between SRAM and DRAM, and explain their reading and writing operation with diagram. [(CO3)(Remember/LOCQ)]

   (b) What is cache mapping? Explain direct mapping for 256 × 8 Ram and 64 × 8 Cache memory. Briefly explain the functionality of an associative memory? [(CO3)(Understand/LOCQ)]

(3 + 3) + (1 + 4 + 1) = 12

Group - E

8. (a) What is a Real Time Operating System (RTOS)? What are the practical challenges involved with implementing a RTOS? How is it different from GPOS? [(CO4)(Remember/LOCQ)]

   (b) The register transfer statements for a register R and the memory in a computer are as follows (the X's are control functions that occur at random)

   X3'X1: R <---M[AR]; Read memory word into R
   X1'X2': R <---AC ; Transfer AC to R
   X1'X3: M[AR] <-- R ; Write R to memory

   Memory has data inputs, outputs, address inputs, and control inputs to read and write. Draw the hardware. [(CO4)(Analyze/IOCQ)]

(2 + 2 + 2) + 6 = 12

9. (a) What are the basic difference between the OS Task, Process, and Threads? [(CO5)(Remember/LOCQ)]

   (b) The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field of the instruction in one memory word. [(CO3)(Analyze/IOCQ)]

(2 + 2 + 2) + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	58.33	31.25	10.42

Course Outcome (CO):

After the completion of the course students will be able to

1. Explain the differences between embedded systems and general computing systems and compare different embedded architectures.
2. Explain the operations of different buses and their uses.
3. Select memory devices as per requirement and design memory and I/O interfacing.
4. Determine the suitable processors/controllers for a design.
5. Design RTOS for an application and assess the performance.
6. Create and fault find embedded systems.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.