LOW POWER HIGH PERFORMANCE DIGITAL VLSI CIRCUIT DESIGN
(ECEN 4221)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) With Technology advancement via contact resistance
(a) Decreases (b) Increases
(c) Remains same (d) Hard to say.

(ii) Average wire delay is changing with Technology advancement in following way
(a) Remaining same (b) Decreasing
(c) Increasing (d) Increasing and then decreasing.

(iii) In Die Variation (IDV) means variation
(a) Within Wafer (b) Inside die
(c) Lot to Lot (d) Wafer to Wafer.

(iv) From 65nm Onwards below power is maximum in a chip
(a) Dynamic (b) Short Circuit
(c) Leakage (d) Contention.

(v) Activity Factor is maximum for below circuit output
(a) Memory Node (b) Dynamic
(c) Static (d) Clock.

(vi) If Threshold Voltage of transistor is increased 2x, Dynamic power of Digital Gate
(a) Remains Same (b) Increases 2x
(c)Decreases 2x (d) Increases 4x.

(vii) If Channel Length of transistor is increased 2x, Channel Leakage of transistor
(a) Decreases 2x (b) Increases 2x
(c) Remains Same (d) Decreases 4x.

(viii) If P_A is Signal Probability of A input of Buffer, the Signal Probability of BufferOutput is
(a) P_A (b) 1- P_A
(c) 1 (d) 0.5.

(ix) The critical path for a design refers to
(a) The path having maximum delay (b) The path with minimum delay
(c) The path with optimum delay (d) The path with no delay.

(x) For a Rising Edge Triggered D-Flip-Flop, if Setup time is 300ps and hold time is 200ps, then input Data needs to be stable for timing window of
(a) 200ps (b) 500ps (c) 300ps (d) 400ps.

Group - B

2. (a) Explain Elmore delay with example. *[(CO3)(Remember/LOCQ)]*
(b) Explain Interconnect coupling noise *[(CO3)(Understand/LOCQ)]*
6 + 6 = 12

3. (a) What is the connection between Static Timing Analysis and LIB (Liberty) File. *[(CO2)(Analyze/IOCQ)]*
(b) In what PVT corner MOS Transistors are fastest and why? *[(CO4)(Evaluate/HOCQ)]*
6 + 6 = 12

Group - C

4. (a) For a flip flop based sequential circuit, Cycle Time = 600ps, Setup Time = 100ps, Clock-Skew = 60ps, Combinational Delay = 470ps, Clock to Out Delay of Flop = 80ps. Hold Time = 170ps. What is setup margin and hold margin for the Circuit? *[(CO2)(Evaluate/HOCQ)]*
(b) Define clock skew and what are sources of Clock Skew? *[(CO4)(Understand/LOCQ)]*
6 + 6 = 12

5. (a) What are various components of Switching Load Capacitance (C_L) in Digital Circuit ? *[(CO5)(Understand/LOCQ)]*
(b) What are various techniques of reducing C_L? *[(CO5)(Understand/LOCQ)]*
6 + 6 = 12

Group - D

6. (a) For 3 input NOR gate, mention leaking transistors (channel leakage) for all possible combination of inputs. *[(CO6)(Evaluate/HOCQ)]*
(b) Explain how both channel and gate leakage can be reduced in FINFET Transistor without compromising delay performance with respect to traditional Transistor? *[(CO6)(Analyze/IOCQ)]*
6 + 6 = 12

7. (a) Sketch the Y chart for simplified VLSI design flow in three domains. *[(CO1)(Remember/LOCQ)]*
(b) Explain difference between Pre-layout and Post Layout timing Verifications. *[(CO1)(Analyze/IOCQ)]*
6 + 6 = 12

Group - E

8. (a) Briefly explain interconnect capacitance components. *[(CO3)(Analyze/IOCQ)]*
   (b) Why driver side of a wire needs to be low resistance and receiver side of the wire needs to be low capacitance, explain using Elmore Delay model. *[(CO3)(Analyze/IOCQ)]*

6 + 6 = 12

9. (a) Write flow chart of VLSI Design and Verification Cycle. *[(CO1)(Remember/LOCQ)]*
   (b) What is parasitic Extraction and Back Annotation? *[(CO1)(Understand/LOCQ)]*

6 + 6 = 12

Cognition Level	*LOCQ*	*IOCQ*	*HOCQ*
Percentage distribution	*50*	*31.25*	*18.75*

Course Outcome (CO):

After the completion of the course students will be able to
1. Learn timing Verification flows
2. Learn Static Timing Analysis Method
3. Learn Interconnect Design
4. Learn Process Variation impact on design
5. Learn Dynamic Power Reduction Techniques
6. Learn Standby Power Reduction Techniques

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*