DIGITAL VLSI DESIGN
(ECEN 3201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The time taken by a square wave to go from 10% to 90% of its final voltage level is called
(a) fan-out (b) rise time
(c) fall time (d) propagation delay.

(ii) The fan-out of a digital circuit means
(a) amount of cooling required by the gate
(b) the number of other gates that can be connected to one of the gate's input
(c) the physical distance between the output pins of the circuit
(d) the number of other gates that can be connected to one of the gate's output.

(iii) Which of the following is true for a NMOS operating in the linear region?
(a) $V_{DS} < (V_{GS}-V_t)$ (b) $V_{DS} > (V_{GS}-V_t)$
(c) $V_{GS} < V_t$ (d) $V_{GS} = 0$.

(iv) Dynamic power dissipation of a CMOS depends on
(a) Channel width of the MOSFETS (b) MOSFET characteristics
(c) Switching frequency (d) Input voltage.

(v) The body or the substrate terminal of a PMOS device is tied to the
(a) negative most supply of the system
(b) positive most supply of the system
(c) generally remains as a dangling terminal
(d) none of the above.

(vi) In a CMOS inverter, the direct current path exists from supply voltage (VDD) to ground when both _____ and _____ are turned ON.
(a) NPN and NMOS (b) PMOS and NMOS
(c) PNP and NPN (d) none of these

(vii) What is the logical effort of "R" number of inputs in a NOR logic gate?
(a) 2R/3 (b) (R+1)/3
(c) (2R+1)/3 (d) None of these.

(viii) Most Manual Effort is needed in which of the below VLSI Methodology?
(a) FPGA (b) Gate Array
(c) Std Cell Based Semi Custom (d) Full Custom.

(ix) Which of the following is considered as an electrical fault?
(a) Excessive steady state current (b) Delay fault
(c) Bridging fault (d) Logical Stuck-at-0 or Stuck-at-1.

(x) The equivalent (W/L) of two nMOS transistors with (W_1/L) and (W_2/L) connected in parallel is
(a) $(W_1/L) + (W_2/L)$ (b) $(W_1/L) \times (W_2/L)$
(c) $[1/(W_1/L) + 1/(W_2/L)]^{-1}$ (d) $(W_1/L) / (W_2/L)$.

Group - B

2. (a) Draw the Voltage Transfer Characteristics of a CMOS inverter for (i) $k_n=k_p$ (ii) $k_n>k_p$, (iii) $k_n<k_p$. Draw the 3VTCs in the same axes frame to clearly indicate the variations. Give proper justification for the graphs. *[(CO1)(Understand/LOCQ)]*

(b) Consider the Boolean form f=Σm(0,1,2,5,6). Realize this with the help of PLA logic design. *[(CO1)(Apply/IOCQ)]*

(4 + 3) + 5 = 12

3. (a) A 64-bit off-chip bus operating at 1 V and 100 MHz clock rate is driving 25 pF/bit capacitance. Each bit is estimated to have a toggling probability of 0.25 at each clock cycle. Calculate the dynamic power dissipation in operating the bus. *[(CO2)(Evaluate/HOCQ)]*

(b) Design a CMOS gate for the logic function f(a,b,c)=Σm(0,1,3,5,6). Mention the widths of NMOS and PMOS for the above design so that the current driving capability remains same as that of the basic CMOS inverter. *[(CO1)(Apply/IOCQ)]*

(c) Briefly discuss about VLSI design flow with the help of a Y-Chart. *[(CO2)(Remember/LOCQ)]*

4 + 6 + 2 = 12

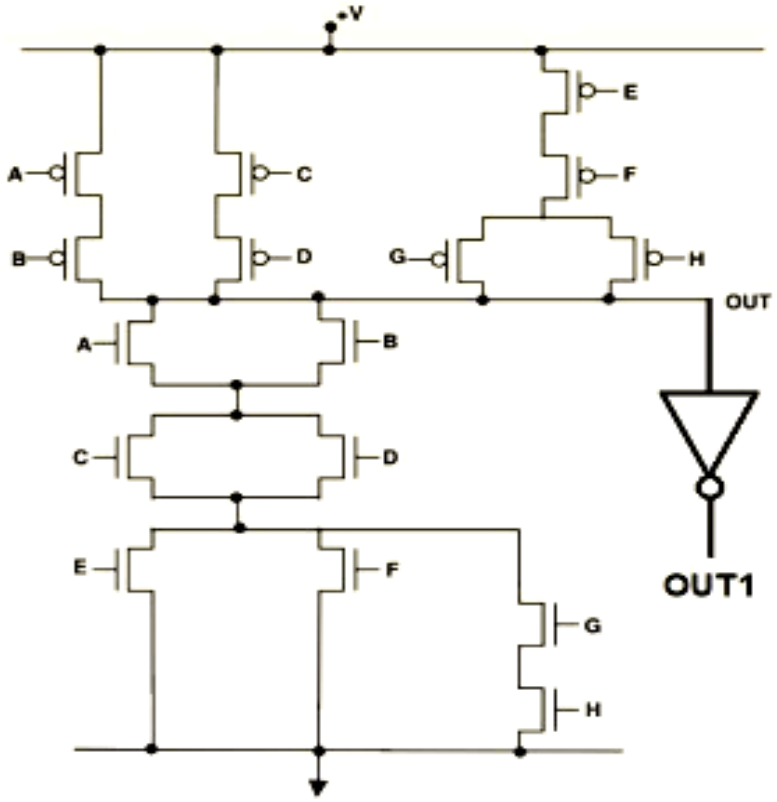
Group - C

4. (a) Draw the stick diagram of the function $Y = \overline{AD + E + BC}$ using Euler Path Algorithm. *[(CO4)(Apply/IOCQ)]*

(b) Explain the Write-1 operation of a 3-Transistor DRAM cell with the help of the circuit diagram. *[(CO4)(Understand/LOCQ)]*

6 + 6 = 12

5. (a) Considering the given CMOS topology, implement the Boolean expression available at the OUT1 node.



[(CO3)(Apply/IOCQ)]

(b) Draw the circuit and timing diagram of a D-latch using Transmission Gate. Briefly state set-up time and hold-time. *[(CO3)(Understand/LOCQ)]*

(c) Realise a 2-input X-NOR gate using transmission gate. *[(CO3)(Apply/IOCQ)]*

3 + 6 + 3 = 12

Group - D

6. (a) Implement the Data Flow Graph of the following function,
x= a*b;
y=a-c;
z=x+d;
x=x*c;
Using Data Flow Graph, realize the data path logic. *[(CO5)(Remember/LOCQ)]*

(b) Write the Verilog code for the structural modelling of a 4:1 multiplexer using three 2:1 multiplexer modules. Draw the complete block diagram of the model. *[(CO5)(Apply/IOCQ)]*

6 + 6 = 12

7. (a) Write the verilog code for designing a sequence counter which will count the following sequence: 0,1,2,5,6,8,10,3,0..... *[(CO5)(Apply/IOCQ)]*

(b) Discuss the significance of Modularity in VLSI Design Methodology. *[(CO2)(Understand/LOCQ)]*

(c) Write a Verilog code for designing a positive edge triggered Mod-16 counter. *[(CO5)(Apply/IOCQ)]*

5 + 3 + 4 = 12

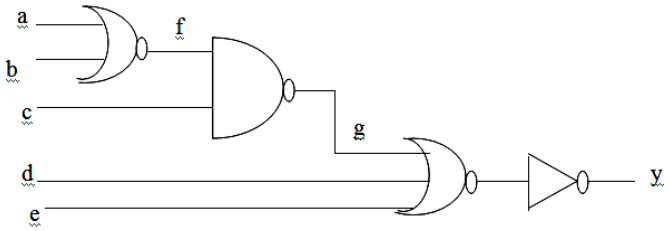
Group - E

8. (a) Explain the different kinds of physical faults that can occur on a CMOS chip and relate them to typical circuit failures. *[(CO6)(Analyze/IOCQ)]*

(b) Explain the different types of Bridging Faults with the help of suitable diagrams. *[(CO6)(Understand/LOCQ)]*

6 + 6 = 12

9. (a) Find the test vector for the following circuit which has got a Stuck-at-0 fault at 'g'



[(CO6)(Evaluate/HOCQ)]

(b) Discuss the 3types of Delay Faults. Briefly state the nature of these faults. *[(CO6)(Analyze/IOCQ)]*

7 + 5 = 12

Cognition Level	*LOCQ*	*IOCQ*	*HOCQ*
Percentage distribution	*37.5*	*51.04*	*11.46*

Course Outcome (CO):

After the completion of the course students will be able to

1. Students will be able to relate to different MOS structures and functions in order to apply the knowledge in building CMOS circuits
2. Students will learn VLSI Design Cycle, Style and Methodology.
3. Students will be able to determine logic and performance of CMOS combinational and Sequential Circuit including Memory Array Design.
4. Students will be able to construct Physical Layout Design and Stick Diagram of Digital Gates.
5. Students will be able to make use of various synthesis flow and HDL modeling in ASIC Semi Custom Design.
6. Students will be able to interpret Si Testing and Debug related algorithms and Fault Modeling.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*