DIGITAL SYSTEMS DESIGN
(ECEN 2202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Which of the following boolean expressions is 'NOT TRUE'?
(a) A + 1 = A (b) A + A′ = 1 (c) A.A = A (d) A.A′ = 0.

(ii) The decimal number 10 is represented in its BCD form as
(a) 10100000 (b) 01010111 (c) 00010000 (d) 00101011.

(iii) The code where all successive numbers differ from their preceding number by single bit is
(a) Alphanumeric Code (b) BCD (c) Excess 3 (d) Gray.

(iv) When both set and reset are disabled in S-R flip flop then the output will be
(a) Set (b) Reset (c) No change (d) Indeterminate.

(v) A modulus -10 Johnson counter requires a minimum of
(a) 10 flip-flops (b) 5 flip-flops (c) 4 flip-flops (d) 12 flip-flops.

(vi) Gray code of $(110101)_2$ is
(a) 101111 (b) 100110 (c) 111010 (d) 101011.

(vii) Race around condition is avoided using
(a) J-K flip flop (b) Faster gates
(c) Look ahead carry generator (d) Edge triggered flip flop.

(viii) An n-stage ripple counter can count up to
(a) 2^n (b) $2^n - 1$ (c) n (d) $2^{(n-1)}$.

(ix) The fastest ADC is
(a) counter-type (b) flash-type
(c) successive-approximation type (d) dual-slope type.

(x) What will be the output from a D flip – flop if the clock is low and D = 0?
(a) 1 (b) 0 (c) No change (d) Toggle between 0 and 1.

Group - B

2. (a) Simplify the Boolean function by using K-map:
F = ∏M(2, 8, 9, 10, 11, 12, 14) and implement the real minimal expression in universal logic. [(CO1)(Evaluate/HOCQ)]
(b) Expand A′ + B′ to minterms and maxterms. [(CO1)(Apply/IOCQ)]
8 + 4 = 12

3. (a) Simplify the given Boolean expression using Quine-McCluskey procedure
f(A,B,C,D)=∑m(0,1,3,6,9,10,11,12,14,15). [(CO1)(Understand/HOCQ)]
(b) Design a 2 bit magnitude comparator circuit using basic gates.
[(CO2)(Analyse/IOCQ)]
6 + 6 = 12

Group - C

4. (a) Design and implement a Full Adder circuit using two Half Adders.
[(CO2)(Analyze/IOCQ)]
(b) What are ROM and RAM? What are the basic differences between EPROM and EEROM? [(CO6)(Remember, Analyze/LOCQ)]
(c) With the help of a logic diagram and a truth table, explain an Octal to Binary encoder. [(CO2)(Apply/IOCQ)]
4 + (2 + 2) + 4 = 12

5. (a) Implement the following function using 8:1 MUX:
F(A, B, C, D)=∑m(1, 3, 4, 11, 12, 13, 14, 15)
[(CO2)(Evaluate/HOCQ)]
(b) Realize a Full Adder Circuit using 3 to 8 Decoder. [(CO2)(Analyze/IOCQ)]
6 + 6 = 12

Group - D

6. (a) Draw the gate level circuit diagram of a positive edge-triggered JK flip-flop and explain its operation with the help of a truth table. How the race around condition eliminated? [(CO3)(Remember/LOCQ)]
(b) What is a shift register? Distinguish between a shift register and a counter.
[(CO3)(Remember/LOCQ)]
(c) Design a 4-bit ring counter using J-K flip-flops. [(CO3)(Create/HOCQ)]
(5 + 2) + (1 + 2) + 2 = 12

7. (a) A clocked sequential circuit has four states A, B, C and D as show in the state diagram of Fig.1. Assume state assignments as A = 00, B = 01, C = 10 and D = 11. Prepare the state table and draw circuit using D flip-flops.
[(CO3)(Understand/HOCQ)]

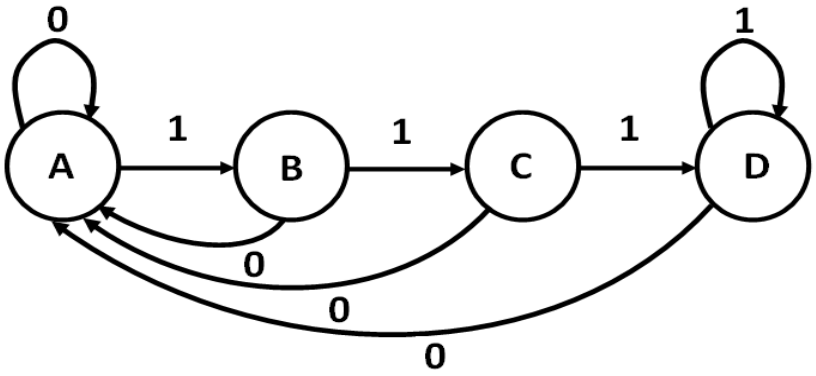

***Fig.1*: State diagram of a clocked sequential circuit**

(b) Design a synchronous MOD 3 UP Counter using J-K flip-flops.
[(CO3)(Analyze/IOCQ)]
6 + 6 = 12

Group - E

8. (a) Explain the operation of Flash type Analog to Digital converter with appropriate circuit diagram. [(CO4)(Remember/LOCQ)]
   (b) Draw and explain the circuit of R-2R ladder type Digital to Analog converter.
   [(CO4)(Remember/LOCQ)]
   6 + 6 = 12

9. (a) With the help of necessary circuit diagram, explain the operation of dual slope type ADC. [(CO4)(Remember/LOCQ)]
   (b) What are the advantages and disadvantages of the Flash type A/D converter?
   [(CO4)(Understand/LOCQ)]
   (c) Design a 2-input NAND gate using CMOS inverter. [(CO5)(Analyze/IOCQ)]
   6 + 2 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	35.42	35.42	29.17

Course Outcome (CO):

1. Make use of the concept of Boolean algebra to minimize logic expressions by the algebraic method, Kmap method, and Tabular method.
2. Construct different Combinational circuits like Adder, Subtractor, Multiplexer, De-Multiplexer, Decoder, Encoder, etc.
3. Design various types of Registers and Counters Circuits using Flip-Flops (Synchronous, Asynchronous, Irregular, Cascaded, Ring, Johnson).

4. Outline the concept of different types of A/D and D/A conversion techniques.
5. Realize basic gates using RTL, DTL, TTL, ECL, and CMOS logic families.
6. Relate the concept of Flip flops to analyze different memory systems including RAM, ROM, EPROM, EEROM, etc.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.