**B.TECH/IT/4TH SEM/INFO 2203 (BACKLOG)/2023**

# COMPUTER ORGANIZATION AND ARCHITECTURE
## (INFO 2203)

**Time Allotted : 3 hrs** **Full Marks : 70**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

## Group – A
### (Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The pipelining process is also called as _____
(a) Superscalar operation (b) Assembly line operation
(c) Von Neumann cycle (d) None of the mentioned.

(ii) The periods of time when the unit is idle is called as _____
(a) Stalls (b) Bubbles
(c) Hazards (d) Both Stalls and Bubbles.

(iii) When the processor executes multiple instructions at a time it is said to use _____
(a) single issue (b) Multiplicity (c) Visualization (d) Multiple issues.

(iv) In super-scalar processors, _____ mode of execution is used.
(a) In-order (b) Post order
(c) Out of order (d) None of the mentioned

(v) The step where in the results stored in the temporary register is transferred into the permanent register is called as _____
(a) Final step (b) Commitment step
(c) Last step (d) Inception step.

(vi) Both the CISC and RISC architectures have been developed to reduce the _____
(a) Cost (b) Time delay
(c) Semantic gap (d) All of the mentioned.

(vii) The BOOT sector files of the system are stored in _____
(a) RAM (b) Hard disk
(c) ROM (d) Fast solid state chips in the motherboard.

(viii) Which of the following technique/s used to effectively utilize main memory?
(a) Dynamic linking (b) Dynamic loading
(c) Both Dynamic linking and loading (d) Address binding.

(ix) An 24 bit address generates an address space of _____ locations.
(a) 248 (b) 16,777,216 (c) 1024 (d) 4096

(x) During the transfer of data between the processor and memory we use _____
(a) TLB (b) Buffers (c) Cache (d) none of the above.

## Group - B

2. (a) Draw and explain a logic circuit arrangement that implements carry look ahead adder. *[(CO2)(Remember/LOCQ)]*
(b) Describe single-precision number using IEEE standard format for floating -point numbers. *[(CO2)(Understand/LOCQ)]*

**6 + 6 = 12**

3. Design a 1-bit ALU which will perform following operations:
(i) Addition (ii) Subtraction (iii) AND (iv) OR (v) NOR (vi) NAND. *[(CO2)(Analyse/IOCQ)]*

**(2 × 6) = 12**

## Group - C

4. (a) Describe the concept of locality of reference. [(CO4) (Remember/LOCQ)]
(b) Describe the classification of ROM. Describe briefly the concept of split cache. *[(CO4)(Understand/LOCQ)]*

**4 + (4 + 4) = 12**

5. (a) What is TLB and PMT, explain with example. *[(CO4)(Understand/LOCQ)]*
(b) Describe the concept of Belady's Anomaly? *[(CO4)(Understand/LOCQ)]*
(c) Consider the following page references and calculate the hit and miss ratio applying LRU and FIFO algorithm (let cache memory has 4 page frames).
4 2 1 5 6 4 3 2 1 4 2 1 *[(CO4)(Apply/HOCQ)]*

**(3 + 3) + 6 = 12**

## Group - D

6. (a) State the design parameters for pipeline processors. *[(CO5)(Remember/LOCQ)]*
(b) Discuss the structure of superscalar pipelines, the data dependence problem, the factors causing pipeline stalling and multi instruction-issuing mechanisms (in-order issue and out-of-order issue) in the context of superscalar pipeline design. *[(CO5)(Analyze/IOCQ)]*

**4 + (2 + 2 + 2 + 2) = 12**

7. (a) Discuss the architecture of a very long instruction word(VLIW) processor with diagram. *[(CO5)(Remember/LOCQ)]*
(b) Discuss the architecture of a vector supercomputer with diagram. *[(CO5)(Understand/LOCQ)]*

**6 + 6 = 12**

## Group - E

8. (a) Describe Flynn's Taxonomy with block diagram. *[(CO6)(Remember/LOCQ)]*
   (b) Differentiate between multiprocessor and multicomputer. *[(CO6)(Analyse/IOCQ)]*
   (c) What are the benefits of using multiprocessor? *[(CO6)(Understand/LOCQ)]*

**6 + 3 + 3 = 12**

9. (a) Write the general characteristics of Uniform Memory Access (UMA) and Non-Uniform Memory Access (NUMA) architecture. *[(CO6)(Remember/LOCQ)]*
   (b) Describe the concept of COMA and NORMA computers. *[(CO6)(Understand/LOCQ)]*

**6 + 6 = 12**

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| *Cognition Level* | *LOCQ* | *IOCQ* | *HOCQ* |
|---|---|---|---|
| *Percentage distribution* | *69.79* | *23.95* | *6.25* |

**Course Outcome (CO):**

After the completion of the course students will be able to

1. Describe and explain the difference between computer organization and computer architecture .
2. Design the ALU for different arithmetical and logical problems and apply the knowledge of different multiplication and division algorithm.
3. Formulate design methodology for using various types of instructions.
4. Differentiate between different Memory hierarchy (Primary, Secondary, Cache). Able to solve different kind of numericals based on memory technologies and page replacement techniques.
5. Differentiate between types of pipeline, hazards and selecting remedial techniques to handle the hazards. able to distinguish between parallel architectures. Compare performance parameters of pipelines and deduce derivations to demonstrate change in performance parameters when branching is introduced. Able to solve numericals based on pipeline concepts.
6. Comparing techniques of ILP, types of CU, types of shared memory architectures. Distinguish between different multiprocessor architectures, Data Flow architecture, RISC and CISC architecture.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question*