MICROPROCESSORS AND MICROCONTROLLER
(AEIE 2205)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) LXI B, 3A21H
MOV A,C
ADD B
DAA
HLT
Write the output of the above program:
(a) A = 62H (b) A = 5BH (c) A = 91H (d) A is unmodified.

(ii) PSW in 8085 microprocessor is
(a) 8 bit (b) 16 bit (c) 4 bit (d) 32 bit.

(iii) Total number of T-states required to execute instruction 'INR M' is
(a) 7 (b) 10 (c) 4 (d) 3.

(iv) In the 8051 the external ROM is selected by using
(a) $\overline{EA}$ (b) $\overline{PSEN}$ (c) RESET (d) ALE.

(v) What will be the content of the accumulator and the status of the carry flag after RAL operation, if the content of the accumulator is BCH and CY is 1?
(a) 79_H, 1 (b) 78_H, 1 (c) FE_H, 0 (d) None.

(vi) In 8086, 20 bit physical address for CS = 2345H and IP = 1000H
(a) 23450H (b) 33450H (c) 12345H (d) 24450H

(vii) The PIC16F877 operates in ..... addressing modes.
(a) 2 (b) 3 (c) 4 (d) 5

(viii) Size of internal data memory in 8051 μC is?
(a) 128 byte (b) 256 byte (c) 2 kB (d) 4 kB.

(ix) Choose the incorrect Mnemonic for Microprocessor 8085, from the following:
(a) LDAX H (b) PUSH PSW (c) XRI FEH (d) All of the above.

(x) If the port address of CWR is 7FH in any 8255A, then the portB Port address would be
(a) 70H (b) 7CH (c) 6FH (d) can't be calculated.

Group – B

2. (a) Write an assembly language program to Set the interrupt masks so that RST5.5 is enabled, RST6.5 is masked, and RST7.5 is enabled. *[(CO2)(Create/HOCQ)]*

(b) Explain the execution procedure of CALL 4321_H instruction which is stored at $D9FE_H$ location. *[(CO2)(Understand/LOCQ)]*

6 + 6 = 12

3. (a) Explain the significance of Status Signals IO/$\overline{M}$, S1, S0 of 8085 microprocessor. *[(CO1)(Remember/LOCQ)]*

(b) Explain how the program control returns to the main program from subroutine when executes the RET instruction within Subroutine? *[(CO2)(Analyze/IOCQ)]*

(c) Draw and explain how IC 74LS373 latches lower byte address information from the multiplexed address data bus. *[(CO1)(Understand/IOCQ)]*

4 + 3 + 5 = 12

Group - C

4. (a) Interface two seven segment common cathode displays through latch 74LS373 with microprocessor 8085 via PPI8255A. Write an ALP to display last two digit of your Autonomy roll no on the seven segment displays. Draw a neat interfacing diagram and explain its operation and decode the port addresses for the selected PPI 8255A. *[(CO5)(Design/HOCQ)]*

(b) Discuss about the required hand shaking signals to configure port A of 8255A as an input port in MODE 1 configuration. *[(CO5)(Understand/LOCQ)]*

(4 + 2 + 2) + 4 = 12

5. (a) Write down all the addressing modes available in 8085 processor with examples. *[(CO2)(Understand/LOCQ)]*

(b) Write an assembly language program to find the number of odd and even numbers from a string of 10 data bytes available between $C100_H$ and $C109_H$. *[(CO2)(Create/HOCQ)]*

5 + 7 = 12

Group - D

6. (a) Explain the EU and BIU of microprocessor 8086 with block diagram? *[(CO3)(Explain/IOCQ)]*

(b) Explain the function of any two from OF, DF, and TF of flag register of microprocessor 8086. *[(CO3)(Understand/LOCQ)]*

(c) Explain with diagram how a 20 bit physical address is generated in 8086 microprocessor. If address of CS = 5505_H and address of IP = 0500_H and BP = 2000H. Find the starting and ending address of CS. *[(CO3)(Solve/IOCQ)]*

(4 + 4)+ 2 + 2 = 12

7. (a) What are the advantages of 8086 processor over 8085 processor? *[(CO3)(Analyze/IOCQ)]*

   (b) Describe the function of instruction queue in 8086 processor. *[(CO3)(Understand/LOCQ)]*

   (c) What is the necessity of memory segmentation in 8086 processor and how it is done? *[(CO3)(Understand/LOCQ)]*

4 + 4 + 4 = 12

Group - E

8. (a) Explain with example the Register Indirect and Indexed Addressing Mode of 8051 μC. *[(CO4)(Remember/IOCQ)]*

   (b) Draw and explain the power on reset circuit for 8051 μC. Also indicate the value of SP Register on RESET. *[(CO4)(Understand/LOCQ)]*

   (c) Explain the operation of the following pins of 8051 μC: (Any two)
   (I) Alternative function of P3.0 and P3.1, (II) XTAL1,2, (III) $\overline{EA}$, and (IV) $\overline{PSEN}$ *[(CO4)(Remember/IOCQ)]*

(2 + 2) + (3 + 1) + (2 × 2) = 12

9. (a) Describe the 128 byte RAM organisation in microcontroller 8051. Also explain what is SFR? *[(CO4)(Remember/LOCQ)]*

   (b) Draw and explain the 8 bit configuration of TMOD and TCON registers of microcontroller 8051. *[(CO4)(Understand/LOCQ)]*

   (c) Compare three important features of PIC16F877 and MCS 8051 microcontrollers. *[(CO4)(Compare/IOCQ)]*

(3 + 2) + (2 + 2) + (3) = 12

Cognition Level	*LOCQ*	*IOCQ*	*HOCQ*
Percentage distribution	*43.75*	*34.38*	*21.87*

Course Outcome (CO):

After the completion of the course students will be able to

AEIE2205.1. Understand the architecture of 8-bit microprocessor (8085A).
AEIE2205.2. Develop the skill in program writing of 8-bit microprocessor (8085A).
AEIE2205.3. Understand the architecture and develop the skill in program writing of 16-bit microprocessor (8086).
AEIE2205.4. Understand the architecture and develop the skill in program writing of microprocessor 8051 and PIC16F877.
AEIE2205.5. Understand the architecture and operation of programmable peripheral device 8255A.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*