COMPUTER ORGANIZATION AND ARCHITECTURE
(CSEN 2202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The Instruction Register contains
(a) the address of the next instruction to be executed
(b) the next instruction to be executed
(c) the address of the current instruction being executed
(d) the current instruction being executed.

(ii) Load 50(R1), R5 is a type of _____ addressing mode.
(a) immediate addressing (b) relative addressing
(c) indexed addressing (d) indirect addressing mode

(iii) Conflict miss can be totally eliminated, in case of
(a) Direct mapping cache (b) Fully associative cache
(c) Set Associative cache (d) Can never be eliminated.

(iv) How many address lines are needed to address each memory location in 4096 × 16 memory chip?
(a) 28 (b) 10 (c) 11 (d)12.

(v) Cycle Stealing happens in case of
(a) Programmed IO (b) Maskable Interrupt
(c) Non-Maskable Interrupt (d) DMA.

(vi) A pipelined processor has 6 stages. For 15 numbers of input tasks, the speedup is
(a) 4.5 (b) 7.5 (c)10.5 (d) 20.

(vii) Periodic refreshing is required in
(a) SRAM (b) DRAM (c) ROM (d) EPROM.

(viii) The total number of 4 × 2 crossbar modules required in a $4^2 \times 2^2$ delta network is
(a) 2 (b) 4 (c) 6 (d) 8.

(ix) The Exchange function E(a_{n-1} …. a_1a_0) is mathematically given by
(a) a_{n-2} …. a_1a_0 a_{n-1} (b) a'_{n-1} …. a_1a_0
(c) $a_0a_na_{n-1}$ …. a_1 (d) a_{n-1} …. $a_1a'_0$
Where a_0,a_1,a_2, …., a_n are binary numbers and the symbol (') denotes the complement

(x) From the entry in a segment table, it is understood that the segment #0 has a base address 220 and length 400 words and the segment #1 has a base address 1000 and length 100 words. What are the physical addresses corresponding to the logical addresses Segment #0, Offset = 128 and Segment #1, Offset = 130 respectively?
(a) 348, 1130 (b) TRAP, 1130
(c) 348, TRAP (d) 1128, 350

Group- B

2. (a) Evaluate the arithmetic statement X = (A*B)/(C-D) in zero, three addresses machine instructions. *[(CO1)(Understand/IOCQ)]*

(b) There are 50 registers, and total 55 instructions available in a general purpose computer. The computer allows only 2-address instructions, where one operand can be a register and another can be a memory location. The memory is byte addressable with 64 KB (Kilo bytes) in size. What will be the minimum number of bits to encode the instruction? Give details of instruction format.
[(CO1)(Analyze/HOCQ)]

(c) Differentiate between Hardwired and Microprogrammed control unit.
[(CO1)(Analyze/IOCQ)]

4 + 4 + 4 = 12

3. (a) In a PC-relative addressing mode, there is a "BR 15" instruction at the word address 102 F_{16} of the memory. If the instruction length is 1 word, what will be the content of the Program Counter after execution of the instruction? (Assume the number 15 in the instruction is in decimal). *[(CO1)(Analyse/IOCQ)]*

(b) Why Indexed Addressing Mode is useful? *[(CO1)(Understand/LOCQ)]*

(c) (i) Which type of Instruction Set Architecture does a RISC have?
(ii) RISC computers are less costly compared to CISC. Why?
[(CO1)(Understand/LOCQ)]

(d) In the following instructions, the destination is at the left of the source registers/ memory locations/ data. Initially, registers R1 and R2 contain 800 and 700 respectively. Memory location 1000 contains 600. Assuming all the number given are in decimal, find out the contents of the (i) registers R2, R3 and R4, after execution of the instructions, (ii) effective address of the memory operand for the LOAD instruction and the (iii) addressing modes in case of each of the following instructions?

MOVE R4, #150
LOAD R3, 50(R1, R4)
ADD R2, R3.

[(CO1)(Evaluate/HOCQ)]

2 + 1 + 2 + 7 = 12

Group - C

4. (a) (i) State one reason why Write-back policy is better than Write-through Policy.
(ii) "In case of Direct Mapping Cache, no replacement policy is required". Justify.
[(CO3)(Understand/LOCQ)]

(b) Briefly describe, with example, one software technique to reduce Cache Miss Rate. *[(CO3)(Remember/LOCQ)]*

(c) A computer has 64 K Words of main memory and 1K Words of cache. The block size is 128 words.
(i) Find out the number of cache lines and the number of memory blocks.
(ii) Draw the address partition, clearly showing the tag bits, cache line bits, and word offset bits for a direct mapped cache. *[(CO3)(Analyze/IOCQ)]*

(d) Consider the following Segment Table.

Segment #	Base Address	Segment Length
0	319_{16}	69_{16}
1	1234_{16}	ADD_{16}

Find out the physical addresses corresponding to the following logical addresses?
(i) $0, 43_{16}$ (ii) $1, BAD_{16}$. *[(CO3)(Evaluate/HOCQ)]*

(e) Mention the steps followed by the CPU, when an external device interrupts the CPU. *[(CO4)(Understand/IOCQ)]*

(1 + 1) + 3 + 3 + 2 + 2 = 12

5. (a) A hierarchical Cache-MS memory has the following specifications:
- Cache access time of 90 ns;
- Main memory access time of 500 ns;
- 80% of memory references are for read and 20% for writes;
- The hit ratio of 0.9 for read accesses and 0.80 for write access for cache.

(i) Compute effective memory access time for read.
(ii) Compute Average memory access times for both read and write considering write through policy. *[(CO3)(Understand/HOCQ)]*

(b) Differentiate between the concept of Memory mapped I/O and I/O mapped I/O. *[(CO4)(Analyze /LOCQ)]*

(c) Explain DMA operation to transfer of block of data between memory and peripherals with diagram? *[(CO4)(Understand/LOCQ)]*

5 + 3 + 4 = 12

Group - D

6. (a) Consider the following Reservation Table.

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X		X	

(i) Draw a neat diagram of the corresponding Pipelined processor, showing the input, output and various stages alongwith the interconnection between the stages.
(ii) Determine the set of Forbidden Latencies, and the Initial Collision Vector.

(iii) Draw the state diagram for scheduling the pipeline, showing the steps for at least one state.
(iv) List all simple cycles and point out the Greedy cycle.
(v) Determine the Minimum Average Latency (MAL) of the pipeline? Find out the lower and upper bounds of MAL. *[(CO2,CO6)(Create,Evaluate/HOCQ)]*

2 + 2 + 3 + 2 + 3 = 12

7. (a) Explain Gather and Scatter instructions in Vector processing. *[(CO5)(Remember/IOCQ)]*
(b) Explain vector chaining and vector stride using examples. *[(CO5)(Remember/IOCQ)]*
(c) What is Strip Mining? *[(CO5)(Remember/LOCQ)]*
(d) Consider a 4 segments pipeline with 10 ns clock period. Find out speedup for 200 tasks. *[(CO2)(Remember/IOCQ)]*

3 + 4 + 2 + 3 = 12

Group - E

8. (a) Illustrate the necessity of data routing in an array processor by showing the execution details to compute
S(k) = $\sum_{i=0}^{k} A_i$ for k = 0, 1, ……, (n-1). *[(CO6)(Analyse/IOCQ)]*
(b) Consider two sorted sequences {10, 21, 47, 89} and {19, 35, 63, 72}. Load these numbers on a linear array of 8 Processing Elements (PEs). With the help of diagrams, show the various operations performed in the Batcher's odd-even merge sort algorithm to sort these numbers in ascending order. *[(CO6)(Apply,Analyse/IOCQ)]*
(c) Taking an example, show how a perfect shuffle can be implemented by a sequence of 'Interchange' operations. *[(CO6)(Analyse/IOCQ)]*

5 + 5 + 2 = 12

9. (a) Describe the Omega and Crossbar interconnection network with diagram. *[(CO5)(Understand/LOCQ)]*
(b) State the factors which affect the performance of an interconnection network. *[(CO5)(Analyze/IOCQ)]*

8 + 4 = 12

Cognition Level	*LOCQ*	*IOCQ*	*HOCQ*
Percentage distribution	*26*	*42.7*	*31.3*

Course Outcome (CO):

After the completion of the course students will be able to

CSEN2202.1 Understand the basic organization of computer and different instruction formats and addressing modes.
CSEN2202.2 Analyze the concept of pipelining, segment registers and pin diagram of CPU.
CSEN2202.3 Understand and analyze various issues related to memory hierarchy.
CSEN2202.4 Understand various modes of data transfer between CPU and I/O devices.
CSEN2202.5 Examine various inter connection structures of multi-processor.
CSEN2202.6 Design architecture with all the required properties to solve state-of-the-art problems.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*