DIGITAL ELECTRONICS
(AEIE 2201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The range of numbers for n-bit signed binary number system in 2's compliment method is
(a) 0 to 2^n-1
(b) -2^{n-1} to $+2^{n-1}$
(c) -2^n to + (2^{n-1} – 1)
(d) -2^{n-1} to + (2^{n-1} – 1).

(ii) Binary equivalent of the Gray code 111001 is
(a) 101101_2
(b) 100110_2
(c) 100101_2
(d) 101110_2.

(iii) A 16:1 Multiplexer will have
(a) 4 selector lines and two output lines
(b) 16 selector lines and one output line
(c) 4 selector lines and one output line
(d) none of the above.

(iv) A flip-flop has
(a) one stable state
(b) two stable states
(c) no stable state
(d) none of the above.

(v) The gates required to build a half adder are
(a) EX-OR gate and NOR gate
(b) EX-OR gate and OR gate
(c) EX-OR gate and AND gate
(d) Four NAND gates.

(vi) Universal logic gates are
(a) AND gate and OR gate
(b) NAND gate and OR gate
(c) AND gate and NOR gate
(d) NAND gate and NOR gate.

(vii) How many flip-flops are required to make a MOD-12 counter?
(a) 12
(b) 6
(c) 5
(d) 4.

(viii) In PLA design, we need
(a) fixed AND array and programmable OR array
(b) fixed AND and OR array
(c) programmable AND and OR array
(d) programmable AND array and fixed OR array.

(ix) The terminal count of a typical modulous-15 binary counter is _____
(a) 1000_2 (b) 1111_2
(c) 1110_2 (d) 1101_2

(x) The logic circuit having highest speed of operation is _____.
(a) TTL (b) ECL
(c) CMOS (d) DTL

Group - B

2. (a) (i) Realize an EX-OR gate by using only NAND gate. *[(CO2)(Remember/LOCQ)]*
(ii) Convert $(D3EA)_{16} = (??)_7$ *[(CO1)(Understand/LOCQ)]*
(b) What is the difference between combinational and sequential circuit? *[(CO3)(Understand/LOCQ)]*
(c) How will you implement 2 bit full subtractor using full adder circuit? *[(CO3)(Apply/IOCQ)]*
4 + 2 + 6 = 12

3. (a) Realize a 16:1 Multiplexer by using 4:1 Multiplexer. *[(CO3)(Understand/LOCQ)]*
(b) Implement the logic function $Y(A,B,C,D) = \sum m(1, 3, 5, 7,9, 13, 15)$ by using 8:1 multiplexer. *[(CO3)(Apply/IOCQ)]*
4 + 8 = 12

Group - C

4. (a) Minimize the logic function
$Y(A,B,C,D,E) = \sum m(0,2,3,5,7,8,10,11,14,15) + \sum d(1,4,6,9)$ by using Karnaugh map. *[(CO3)(Understand /LOCQ)]*
(b) Design a J-K flip flop with characteristic table. *[(CO4)(Understand/LOCQ)]*
8 + 4 = 12

5. (a) A negative edge trigerred D flip-flop can work as master-slave flip-flop. Justify with proper explanation. *[(CO4)(Understand/LOCQ)]*
(b) Implement a D- flip flop with truth table by using only NAND gates. *[(CO4)(Apply/IOCQ)]*
6 + 6 = 12

Group - D

6. (a) Design a MOD-16 synchronous counter and explain with output waveforms. *[(CO4)(Create/HOCQ)]*

(b) Design a ripple counter to start the count at 2 and stop the count at 4 and start the count again from 2. *[(CO4)(Create/HOCQ)]*

6 + 6 = 12

7. (a) Write short note on Ring counter. *[(CO4)(Remember/LOCQ)]*
   (b) Implement the given functions using programmable logic array (PLA)
   $X(a, b, c)= \sum m(0, 2, 3, 4)$ $Y(a, b, c)= \sum m(1, 3, 4, 5, 7)$. *[(CO5)(Apply/IOCQ)]*

4 + 8 = 12

Group - E

8. (a) Compare between logic families: TTL, ECL, and CMOS. *[(CO6)(Analyze/IOCQ)]*
   (b) Write short notes on Flash type ADC and Binary weighted DAC. *[(CO5)(Remember/LOCQ)]*

6 + 6 = 12

9. (a) Implement the following logic functions by using PROM:
   $W= \sum(1,3,5,7)$, $X= \sum m(2,4,5,8)$, $Y= \sum m(0,2,3)$ *[(CO5)(Apply/IOCQ)]*
   (b) Design and explain the operation of NAND gate using CMOS logic. *[(CO6)(Understand/LOCQ)]*

6 + 6 = 12

Cognition Level	*LOCQ*	*IOCQ*	*HOCQ*
Percentage distribution	*52.08*	*35.41*	*12.5*

Course Outcome (CO):

After the completion of the course students will be able to

1. Understand the fundamentals of converting from one number system to another.
2. Explain the basic logic operations of NOT, AND, OR, NAND, NOR, and XOR.
3. Analyze, design and implement combinational logic circuits.
4. Analyze, design and implement sequential logic circuits.
5. Describe the nomenclature and technology in the area of memory devices: ROM, PROM, PLD etc. and different kind of ADCs and DACs.
6. Understand the basic electronics of logic circuits and be able to use integrated circuit packages.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*