M.TECH/VLSI/1ST SEM/VLSI 5142/2020

MODELLING OF VLSI DEVICE
(VLSI 5142)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The Fermi level throughout of a PN junction in thermal equilibrium is
(a) constant (b) different
(c) broadened (d) narrowed.

(ii) The contact potential of a PN-junction depends on
(a) Intrinsic carrier concentration
(b) doping concentration
(c) absolute temperature
(d) all of the above.

(iii) With an increase in the drain bias the pinch-off point of a MOSFET shifts towards the
(a) source (b) drain (c) gate (d) substrate.

(iv) The dominant current component in a MOSFET under strong inversion is
(a) drift (b) diffusion
(c) leakage current (d) drift and diffusion both.

(v) The effective channel length of a MOSFET in saturation decreases with increase in the
(a) Gate voltage (b) drain voltage
(c) source voltage (d) substrate voltage.

(vi) The minimum value of the body- effect coefficient of a MOSFET is
(a) zero (b)unity (c)ten (d)100.

(vii) The MOSFET in its linear region of operation behaves like a
(a) resistor (b) capacitor
(c) inductor (d) diode.

(viii) Presence of substrate bias causes the threshold voltage of an NMOS to
(a) increase (b) decrease
(c) remain unaltered (d) go to zero.

(ix) HiSIM model is an example of
(a) SP model (b) CB model
(c) Vth model (d) none of the above.

(x) The collector voltage at which the linearly extrapolated collector current of a BJT reaches zero is known as the
(a) early voltage (b) threshold voltage
(c) cut-off voltage (d) cut-in voltage

Group – B

2. (a) What are the capacitances associated with a PN-junction? Explain their origin.

(b) Explain the mechanism of drift of carriers in a semiconductor. Hence obtain an expression for the conductivity of a semiconductor sample due to drift of both electrons and holes.

6 + 6 = 12

3. (a) Derive the necessary relation to prove that the Fermi level difference is the driving force for the flow of current in a semiconductor.

(b) Mention the ways in which carriers move in a PN-junction. Write down the current- voltage relation of a PN-junction diode.

6 + (4 + 2) = 12

Group – C

4. (a) Draw the band diagram of an n-MOSFET under inversion. Why is the channel called 'inverted'?

(b) Derive the expression of the threshold voltage of an NMOS considering its surfaces to be real.

4 + 8 = 12

5. (a) Justify the nature of variation of the MOSFET capacitance with the applied gate voltage. Give suitable diagram.

(b) How does the substrate bias affect the threshold voltage of a MOSFET?

(5 + 3) + 4 = 12

Group – D

6. (a) Show the effect of full scaling on the following MOSFET parameters: intrinsic delay, power dissipation, power dissipation density and the packing density.

(b) Write a short note on ITRS specifications.

8 + 4 = 12

7. (a) Explain the dependence of threshold voltage on the length of a MOSFET. How can the threshold voltage roll-off in short channel MOSFETs be taken care of?

(b) How are 'hot' electrons created in short channel devices? Discuss the vertical and lateral hot electron effects.

(4+2) + (2+4) = 12

Group – E

8. (a) What is a compact model? Justify the need for the development of compact MOSFET models.

(b) Discuss the Level 1 MOSFET model and its accuracy.

(3+4) + 5 = 12

9. (a) Explain the charge sharing model in a MOSFET.

(b) Mention the important assumptions and the region of its validity of the GCA model of a MOSFET.

8 + 4 = 12

Department & Section	Submission Link
VLSI	https://classroom.google.com/w/MjIxODI4NDkyMzc0/tc/MjkxNDM5MTY0MTE4