# DIGITAL VLSI IC DESIGN
## (VLSI 5101)

**Time Allotted : 3 hrs** **Full Marks : 70**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

## Group – A
## (Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The value of "Lambda" in 0.25um Technology is
(a) 0.25um (b)0.5um (c)1um (d) 0.125um.

(ii) An ideal current source has a resistance value of
(a) 0 ohm (b) Infinite (c)100 Kohm (d)100 ohm.

(iii) The most noise immune among the logic family is
(a) NMOS (b) Pseudo NMOS
(c) Dynamic (d) CMOS.

(iv) The KL Algorithm is related to
(a) Routing (b) Partitioning
(c) Logic synthesis (d) High level synthesis.

(v) Memory design is normally done using the method of
(a) Full custom (b) Std Cell based semi custom
(c) Gate array (d) FPGA.

(vi) The NMOS transistor in linear region can be modelled as
(a) Resistance (b) Current source
(c) Short circuit (d) Voltage source.

(vii) With decrease of $V_{dd}$, the delay of a CMOS inverter shall
(a) Increase (b) Decrease
(c) Remain same (d) Decrease and then increase.

(viii) The minimum number of transistors used in the CMOS logic Y = A + CD is
(a) 12 (b) 6 (c) 8 (d)10.

(ix) A Pentium 4 chip belongs to the category of
(a)VLSI (b)LSI (c) ULSI (d) GSI.

(x) BDD is used in
(a) High level synthesis (b) Logic synthesis
(c) Floorplan (d) Routing

## Group – B

2. (a) What are the various capacitance components of a MOS Transistor?

(b) Draw the VTC (Voltage Transfer Curve) of a CMOS Inverter.

(c) How the VTC of CMOS inverter will change if the width of PMOS is increased ?

(d) For a CMOS Inverter, given the parameters
VOH = 5V, VOL = 0V, $V_{IH}$ = 3.7V, $V_{IL}$ = 2.1V, what are the values of $NM_H$ and $NM_L$?

**4 +3 + 3 + 2 =12**

3. (a) Draw the circuit diagram of a D-Latch using CMOS Transmission Gate (TG).

(b) Draw the circuit diagram of a Positive Edge Triggered D-Flip Flop using D-Latch.

(c) Draw Circuit Diagram of 2 input XOR gate using CMOS Logic.

(d) Draw Circuit Diagram of 2 input XOR gate using CMOS Transmission Gate (TG).

**3+ 3+ 3 + 3 = 12**

## Group – C

4. (a) Draw the Y Chart for VLSI Design.

(b) Draw flow diagram of the VLSI Design Cycle.

(c) Write the VHDL behavioural model for a D – Flip Flop

**5+ 3 + 4 = 12**

5. (a) Solve Euler Path Algorithm for the function f = (CD(A + B)) ! (! Means Bar).

(b) Draw Stick diagram accordingly.

(c) Describe difference between behavioural and structural Model of VHDL coding using an example.

**4+ 4 + 4 = 12**

## Group – D

6. (a) Draw flow diagram of high level synthesis.

(b) Draw flow diagram of logic synthesis.

(c) Draw BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using ordering of a < b< c.

(d) Create ROBDD diagram and corresponding optimized boolean expression.

**3 +3 + 3 + 3=12**

7. (a) Draw flow diagram of Physical Layout Automation.

(b) For floor-planning problem, what are inputs, outputs and objective (cost) function?

(c) Explain Lee Algorithm of Maze Routing.

**4 +4 + 4=12**

## Group – E

8. (a) What are the key limitations of a pseudo-NMOS logic family ?

(b) Why CMOS Transmission gate is used instead of NMOS pass transistor logic?

(c) Draw circuit diagram of a negative edge triggered D-Flip Flop.

(d) Draw circuit diagram of 8 input OR gate using Domino Circuit.

**2+2+4+4=12**

9. (a) Draw flow diagram of Physical Layout Automation

(b) For below Channel Routing problem, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG)
Terminal connection is as follows:
11122563040 ----- Upper Boundary
25055330604 ----- Lower Boundary
0 means no Connection.
Assume HV Layer (V = Metal 1, H = Metal 2)

(c) Provide optimum channel routing solution for above case using Left Edge Algorithm.

**2+ 5 + 5 =12**

| Department & Section | Submission Link |
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| VLSI | https://classroom.google.com/c/MjIxMzQ4OTI0NzQ1/a/MjcxNTEzNDczNzYw/details |