B.TECH / IT / 5TH SEM / INFO 3102 (BACKLOG) / 2020

COMPUTER ARCHITECTURE
(INFO 3102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The pipelining process is also called as _____
(a) Superscalar operation (b) Assembly line operation
(c) Von Neumann cycle (d) None of the mentioned

(ii) The periods of time when the unit is idle is called as ____
(a) Stalls (b) Bubbles
(c) Hazards (d) Both Stalls and Bubbles

(iii) When the processor executes multiple instructions at a time, it is said to use _____
(a) single issue (b) Multiplicity
(c) Visualization (d) Multiple issues

(iv) In super-scalar processors, _____ mode of execution is used.
(a) In-order (b) Post order
(c) Out of order (d) None of the mentioned

(v) The step where in the results stored in the temporary register is transferred into the permanent register is called as _____
(a) Final step (b) Commitment step
(c) Last step (d) Inception step

(vi) Both the CISC and RISC architectures have been developed to reduce the _____
(a) Cost (b) Time delay
(c) Semantic gap (d) All of the mentioned

(vii) The BOOT sector files of the system are stored in ____
(a) RAM (b) Hard disk
(c) ROM (d) Fast solid state chips in the motherboard

(viii) Which of the following technique/s used to effectively utilize main memory?
(a) Dynamic linking (b) Dynamic loading
(c) Both Dynamic linking and loading (d) Address binding.

(ix) An 24 bit address generates an address space of _____ locations.
(a) 248 (b) 16,777,216
(c) 1024 (d) 4096

(x) During the transfer of data between the processor and memory we use _____
(a) TLB (b) Buffers
(c) Cache (d) none of the above

Group – B

2. (a) Describe various computer architectures based on Flynn's classification.

(b) Describe how performance factors are influenced by system attributes in computer architecture.

6 + 6 = 12

3. (a) State the differences between asynchronous and synchronous linear pipelines. Explain the concept of MAL(Minimum Average Latency).

(b) Describe three possible dependencies in a pipelined processor.

(2 + 4) + 6 = 12

Group – C

4. (a) Explain following properties in the context of memory hierarchy.
(i) Inclusion (ii) Coherence (iii) Locality.

(b) Describe cache implementation using direct, fully associative and set associative mapping.

6 + 6 = 12

5. (a) Explain the concept of Translation Lookaside Buffer(TLB), paged memory and segmented memory in the context of virtual memory.

(b) Explain LRU,OPT and FIFO page replacement policies with example.

6 + 6 = 12

Group – D

6. (a) Describe how superscalar processors facilitate instruction level parallelism.

(b) Describe the architecture of VLIW processor and its pipeline operations with diagram.

6 + 6 = 12

7. (a) Describe the working principle and pipeline execution of the vector processor with diagram.

   (b) Describe hardwired and micro programmable control units with diagram.

6 + 6 = 12

Group – E

8. (a) Describe three shared memory multiprocessor models.

   (b) Describe the concept of distributed memory multicomputer system with diagram.

6 + 6 = 12

9. (a) Describe characteristics of the RISC and CISC architectures with diagram.

   (b) Explain the following dynamic connection networks.
   (i) Bus systems
   (ii) Multistage Interconnection Networks(MIN)
   (iii) Crossbar switch networks.

6 + 6 = 12

Department & Section	Submission Link
IT	https://classroom.google.com/c/MjgyNjc1MzY3MTEw/a/MjgyNjgxMzMwMjUw/details