COMPUTER ORGANIZATION
(INFO 2102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Most of time, computer instructions are divided into
(a) function code (b) instruction code
(c) operand (d) both A and C

(ii) Which architecture involves both the volatile and the non volatile memory?
(a) Harvard architecture (b) Von Neumann architecture
(c) None of the mentioned (d) All of the mentioned

(iii) In case of, Zero-address instruction method the operands are stored in _____
(a) Registers (b) Accumulators
(c) Push down stack (d) Cache

(iv) MOV B, A is
(a) Immediate Addressing (b) Register Addressing
(c) Direct Addressing (d) Indirect Addressing

(v) "Delayed Branching " is related to
(a) pipeline hazard (b) pipeline remedy
(c) both a & b (d) none of these

(vi) DVD writer is a
(a) semi random (b) serial
(c) random (d) non- serial access memory.

(vii) The addressing mode, where you directly specify the operand value is _____
(a) Immediate (b) Direct
(c) Definite (d) Relative

(viii) For converting virtual address into physical address, the programs are divided into
(a) Pages (b) Frames
(c) Segments (d) Blocks

(ix) The addressing mode/s, which uses the PC instead of a general purpose register is _____
(a) Indexed with offset (b) Relative
(c) direct (d) both Indexed with offset and direct

(x) How many address lines are needed to address each memory location in 2049×4 memory chip?
(a) 2 (b) 48
(c) 12 (d) 24

Group – B

2. (a) What is Von-Neumann bottleneck? What is the solution of this? Computer organization comes after computer architecture-------Justify.

(b) Why "Relative addressing" is very much popular in programming? Explain with example.

(3 + 2 + 3) + 4 = 12

3. (a) Evaluate (A+B/C)*(G*F) with the help of three, two, one, zero address instruction.

(b) State the difference between "Instruction Register" and "Instruction Buffer Register". Why Program Counter is used?

8 + (2 + 2) = 12

Group – C

4. (a) Prove that final carry in carry look ahead adder is only dependent on the carry generated in first adder.

(b) What is normalized floating point number? Convert 1101011 to IEEE single precision format.

6 + (2 + 4) = 12

5. (a) Multiply -13 and 7 with the help of Booth Multiplication algorithm.

(b) Draw the flow chart of Restoring type of division algorithm. Divide 8 by 3 with the help of Non restoring type of division algorithm.

6 + (3 + 3) = 12

Group – D

6. (a) "Set Associative Mapping is combination of Associative Mapping and Direct Mapping Technique"----justify.

(b) Show the BUS connection with a CPU to connect four RAM chips of size 256×8 bits each and a ROM chip 512×8 bit size. Assume the CPU has 8 bit data bus and 16 bit address bus. Clearly specify generation of chip select signals.

6 + 6 = 12

7. (a) Calculate hit ratio for the following page references using FIFO and frame size 5.
7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1
What is Belady's anomaly?

(b) According to the information, determine the number of bits of the subfields in the address for direct mapping, associative mapping and Set Associative Mapping cache schemes.
Main memory size: 256 MB
Cache memory size: 1 MB
Address space of the processor: 256 MB
Block size: 128 bytes
There are 8 blocks in a set.

(4 + 2) + 6 =12

Group – E

8. (a) Explain relative advantages and disadvantages of pipeline architecture over non pipeline architecture.

(b) Discuss on different type of pipeline hazards.

6 + 6 = 12

9. (a) What is interrupt? Differentiate between interrupt and polling.

(b) Briefly explain the working principle of DMA. What is cycle stealing?

(2 + 3) + (4 + 3) = 12

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IT	https://classroom.google.com/c/Mjk2NTE4NDUxODU4/a/Mjk2NTMzMjgwMzQ0/details