B.TECH / IT / 3RD SEM / INFO 2101 (BACKLOG) / 2020

DIGITAL ELECTRONICS
(INFO 2101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) In which of the following base systems 124 is not a valid number?
(a) Base 10 (b) Base 4
(c) Base 8 (d) Base 16

(ii) An AND gate will function as OR gate if
(a) all the inputs are 1
(b) all the inputs are 0
(c) all the inputs and outputs are complemented
(d) either of the inputs is 1

(iii) A flip-flop circuit can be used for _____.
(a) scaling (b)Counting
(c) demodulation (d) modulation

(iv) Which circuit is used in between two systems having two different codes?
(a) Sequential (b) Combinational
(c) Converter (d) Both a and b

(v) The number of FFs required in a mod-6 counter is _____.
(a) 3 (b) 4
(c) 5 (d) 6

(vi) Which logic is a basic comparator?
(a) XNOR (b) XOR
(c) NAND (d) NOR

(vii) Find the base r of the number system where $(24)_{10} = (33)_r$ is true.
(a) 8 (b) 5
(c) 7 (d) 6

(viii) How many select lines contained in a MUX with 512 input and 1 output line?
(a) 8 (b) 9
(c) 1 (d) 512

(ix) The code used for labelling cells of k-map is
(a) Gray code (b) Octal code
(c) BCD (d) Binary code

(x) The terms which cannot be combined further in the tabular method are called
(a) Implicants (b) Prime implicants
(c) Essential prime implicants (d) Selective prime implicants

Group – B

2. (a) Convert the following Excess 3 code into binary number :
1001, 1011.

(b) Reduce the following logic function using mapping the expression :
$f=\sum m\,(0,1,2,3,5,7,8,9,10,12,1,3)$.

(c) Add the following BCD numbers: 00011001 and 00010100

3 + 6 + 3 = 12

3. (a) Minimize the following expression using Boolean algebra:
(i) $f= (A + B) (A + C') + A'B' + A'C'$
(ii) $f= (B + BC) (B + B'C) (B + D)$

(b) Design a logic circuit that performs 4-bit BCD to Excess-3 code conversion.

(4 + 4) + 4 = 12

Group – C

4. (a) Design a JK flip-flop using D flip-flops.

(b) Implement the following logic function using 8x1 MUX :
$F(A,B,C,D)=\sum m(1,3,4,5,11,12,14,15)$.

6 + 6 = 12

5. (a) Implement the following switching function using multiplexer
$F(w,x,y,z)= \sum m(0,7,11, 15) + \sum d(2,3,4,13)$.

(b) Realize 4:1 multiplexer using only 2:1 multiplexers.

6 + 6 = 12

Group – D

6. (a) Design a synchronous MOD-7 counter using JK FF.

(b) Realize JK Flip Flop using SR Flip Flop.

7 + 5 = 12

7. (a) Design a counter with count sequence 0,2,4,6,0,2.... and repeat using JK FFs.

(b) Differentiate synchronous and asynchronous counter.

10 + 2 = 12

Group – E

8. Design a sequence detector which detects the sequence 1011 using D flip flop.

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9. Design an asynchronous circuit that has two inputs X1 and X2 and one output Z. The circuit is required to give an output whenever the input sequence (0, 0) (0, 1) and (1, 1) is received but only in that order.

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Department & Section	Submission Link
IT	https://classroom.google.com/c/MjEyMzAyOTQ3NDM5/a/MjEyMzAxMzIzMzgz/details