RF IC DESIGN AND MEMS
(VLSI 6132)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) SFDR is the specification for
(a) DAC (b) ADC (c) Both DAC & ADC (d) All RFIC.

(ii) The *S*-parameter (S_{22}) characterizes
(a) gain (b) reverse isolation
(c) Input matching of the two-port network (d) output matching.

(iii) Due to skin effect, the resistance of a trace will
(a) decrease (b) increase (c) remain unchanged (d) none of the above.

(iv) The stern stability factor for LNA is defined as
(a) $K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|}$ (b) $K = \frac{1+|\Delta|^2+|S_{11}|^2+|S_{22}|^2}{2|S_{21}||S_{12}|}$
(c) $K = \frac{1+|\Delta|^2-|S_{21}|^2-|S_{12}|^2}{2|S_{11}||S_{22}|}$ (d) $K = \frac{1+|\Delta|^2+|S_{21}|^2+|S_{12}|^2}{2|S_{11}||S_{22}|}$

(v) Port-to-port feed through in mixer is created by
(a) gate-source capacitance (b) gate-drain capacitance
(c) both (a) & (b) (d) none of the above.

(vi) Shannon's theorem states that the achievable data rate of a communication channel is equal to
(a) $2B \log_2(1 + SNR)$ (b) $B \log_2(1+SNR)$
(c) $(B/2) \log_2(1+SNR)$ (d) $B \log_2(1+2SNR)$
where, *B* denotes bandwidth and *SNR* the signal-to-noise ratio.

(vii) The "image" frequency of a desired signal is given by
(a) $\omega_{im} = \omega_{in} + 2\omega_{IF}$ (b) $\omega_{im} = \omega_{in} - 2\omega_{IF}$
(c) $\omega_{im} = 2\omega_{in} + \omega_{IF}$ (d) $\omega_{im} = 2\omega_{in} - \omega_{IF}$.

(viii) Anodic bonding of a silicon/gas substrate takes place under
(a) high temperature (b) high pressure
(c) high temperature & pressure (d) high temperature & high electric voltage.

(ix) The term LIGA refers to
(a) design (b) material
(c) microfabrication process (d) none of these.

(x) SOI stands for
(a) splitting of ions (b) silicon on insulator
(c) substrate on insulator (d) silicon orientation index.

Group- B

2. (a) Explain the principle of operation of varactors. [(CO6)(Understand /LOCQ)]

(b) An analog multiplier "mixes" its two inputs $x_1(t) = A_1 cos\ \omega_1 t$ and $x_2(t) = A_2 cos\ \omega_2(t)$ and ideally produces $y(t) = kx_1(t)x_2(t)$, where k is a constant. If the mixer is ideal, determine the output frequency components. If the input port sensing $x_2(t)$ suffers from third-order nonlinearity, determine the output frequency components. [(CO1)(Apply/IOCQ)]

(c) We wish to employ a capacitive coupling at the input of a stage (*Fig. 1*) that as an input capacitance of C_{in}. Determine the additional input capacitance resulting from the coupling capacitor. Assume, $C_p = 0.1C_c$. [(CO6)(Evaluate/HOCQ)]]

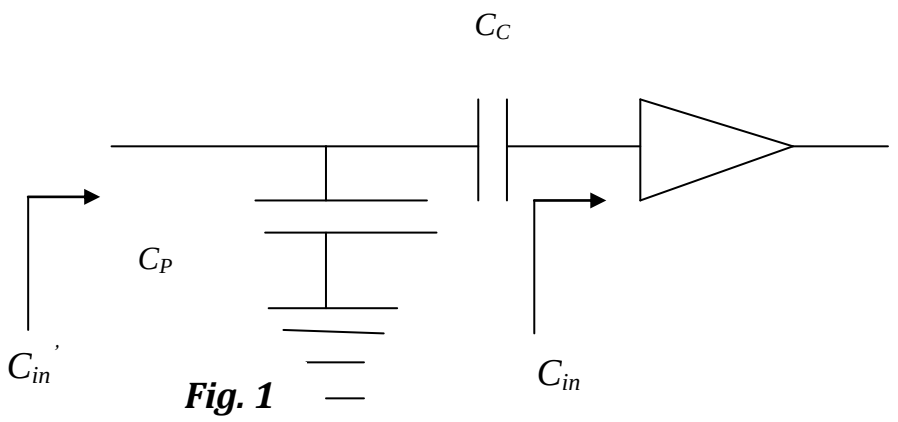

Fig. 1

4 + 5 + 3 = 12

3. (a) Explain "current crowding" effect in spiral inductor geometry. [(CO6)(Understand/LOCQ)]

(b) Estimate the effect of parasitic capacitance to the substrate and interwinding capacitance of a spiral inductor with mathematical modelling. [(CO6)(Apply/IOCQ)]

(c) Determine the noise figure of the cascade of common-source stages shown in Fig. 2. Neglect the transistor capacitances and flicker noise. [(CO1)(Evaluate/HOCQ)]

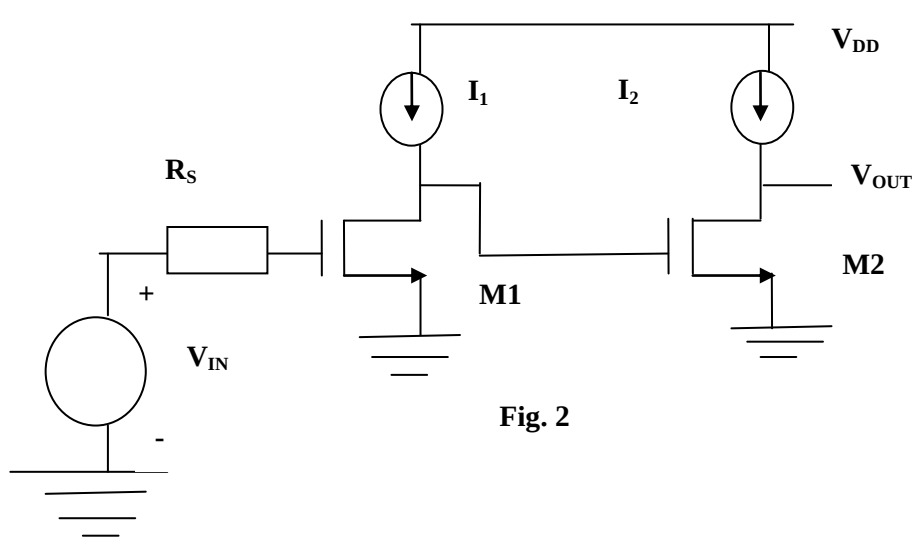

Fig. 2

4 + 5 + 3 = 12

Group – C

4. (a) Explain the principle of operation of dual down conversion heterodyne receiver. [(CO2)(Understand/LOCQ)]

(b) Down conversion to what minimum intermediate frequency avoids self-corruption of asymmetric signals? [(CO2)(Analyze/IOCQ)]

(c) A student decides to omit a pre-driver and simply "scale-up" the up-converter so that it can drive the power amplifier directly. Justify the drawback of this approach. [(CO6)(Evaluate/HOCQ)]

4 + 5 + 3 = 12

5. (a) Briefly discuss the noise and linearity issues of a mixer in a transceiver. [(CO3)(Understand/LOCQ)]

(b) Derive the expression of voltage gain, output impedance and noise figure of the common-source stage with resistive feedback *LNA* topology. [(CO3)(Analyze/IOCQ)]

(c) Determine the noise figure of the stage (Fig. 3) with respect to a source impedance of R_S. Neglect channel-length modulation and body effect. [(CO3)(Evaluate/HOCQ)]

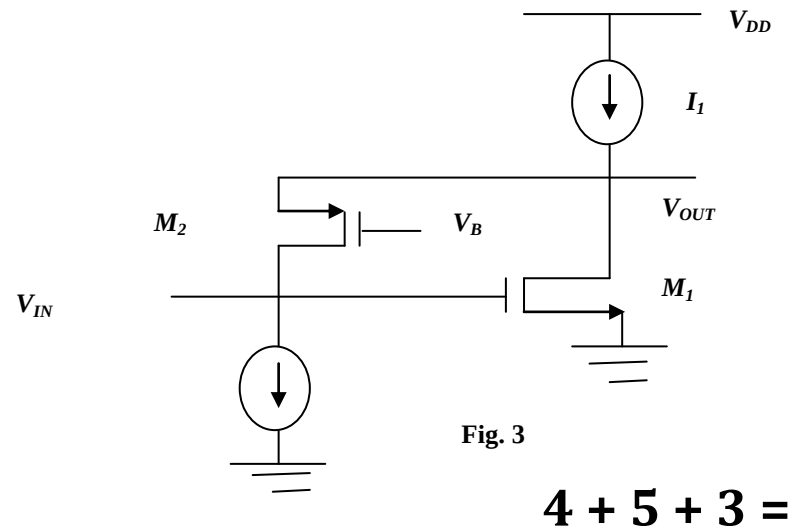

Fig. 3

4 + 5 + 3 = 12

Group - D

6. (a) Discuss the steps of Bulk Micromachining with proper diagrammatic illustrations. [(CO4)(Understand/LOCQ)]

(b) Discuss in detail how the CVD process can be utilized during the fabrication of Microsystems. [(CO5)(Understand/LOCQ)]

6 + 6 = 12

7. (a) Compute the Miller indices of a plane which has intercepts of (3,5,6) in the (a,b,c) crystallographic axes respectively. [(CO4)(Apply/IOCQ)]

(b) Illustrate on: (i) Isotropic etching (ii) MEMS pressure sensor. [(CO4)(Apply/IOCQ)]

(c) Classify the different processes of actuation. [(CO4)(Analyse/IOCQ)]

2 + 6 + 4 = 12

Group - E

8. (a) Describe the working principle and structure of a piezoresistive pressure sensor. [(CO6)(Analyze/IOCQ)]

(b) Explain micromechanical resonators. Review the alterations that can be made in the MEMS resonator to increase its resonant frequency. [(CO4)(Analyze/IOCQ)]

6 + (3 + 3) = 12

9. (a) Realize the steps of realizing cantilever structure by surface micromachining process. [(CO5)(Remember/LOCQ)]

(b) Draw a neat diagram of a surface micro-machined variable capacitor. Explain its working principle. [(CO6)(Apply/IOCQ)]

(c) What are the desirable properties in an rf micromechanical switch? [(CO6)(Analyze/IOCQ)]

4 + (3 + 3) + 2 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	33.33	54.17	12.50

Course Outcome (CO):

After the completion of the course students will be able to

1. Specify noise and interference performance metrics like noise figure, IIP3 and different matching criteria.
2. Comprehend different multiple access techniques, wireless standards and various transceiver architectures.
3. Design various constituents' blocks of RF receiver front end.
4. Describe MEMS fabrication technologies.
5. Critically analyze micro-systems technology for technical feasibility as well as practicality.
6. Comprehend the working of various systems and design electronic circuits for various applications.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question