EMBEDDED SYSTEMS DESIGN
(VLSI 5102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The locality of reference justifies the use of
(a) Flash memory (b) Cache Memory (c) Main memory (d) Virtual memory.

(ii) Primary agent responsible for correct working of an embedded system is
(a) GPOS (b) RTOS (c) UNIX (d) Windows.

(iii) A phototransistor is a _____ and a LED is an _____ .
(a) actuator, sensor (b) sensor, actuator (c) actuator, actuator (d) sensor, sensor.

(iv) Inter Integrated Circuit Bus protocol is a _____ communication protocol.
(a) parallel (b) serial (c) message-passing (d) FM.

(v) The logic family, which takes the least power is
(a) TTL (b) RTL (c) CMOS (d) ECL.

(vi) Which is not an embedded processor?
(a) ARM 7 (b) ARM 9 (c) AMD 29050 (d) IBM 370.

(vii) The number of active elements in a DRAM cell is
(a) 1 (b) 2 (c) 6 (d) 9.

(viii) In microcontroller 8051 the program status word bits 4 and 3 are
(a) Register Bank selector bits 0 and 1 (b) Unused
(c) Register Bank selector bits 1 and 0 (d) CY flag and Zero flag.

(ix) A logic circuit in ALU is
(a) Entirely combinational (b) Entirely sequential
(c) Both (a) and (b) (d) Purely passive.

(x) Concept of refreshing the memory content periodically is used by
(a) SRAM (b) DRAM
(c) FLASH (d) All of the above.

Group - B

2. (a) Given a 32X8 ROM with an enable input, show the external connections necessary to construct 128X8 ROM with four chips and a decoder. [(CO1)(Remember/LOCQ)]

   (b) Consider the following register transfer statements for two four bit registers R1 and R2

   xT : R1 ← R1+R2

   x'T : R1 ← R1

   Draw a hardware implementation of the two statements using two registers, a 4 bit adder and a quadruple 2 to 1 line multiplexer. [(CO1)(Understand/LOCQ)]

   6 + 6 = 12

3. (a) Explain, with examples, what is a real-time system? What are the differences between a RTOS and a GPOS? [(CO2)(Analyze/IOCQ)]

   (b) Explain real-time classification as "hard", "firm" and "soft" with examples. Where would one categorize the "Automatic Flight Control of air plane"? [(CO2)(Analyze/IOCQ)]

   6 + 6 = 12

Group - C

4. (a) What is Harvard architecture? Explain briefly using block diagram. [(CO3)(Apply/IOCQ)]

   (b) Explain ARM Cortex 8 instructions Fetch Decode unit and Execute unit. [(CO3)(Apply/IOCQ)]

   (c) A 4 stage pipeline system takes 20 ns to process a sub operation in each stage. The pipeline executes 10 tasks in sequence. What is the speed up ratio? [(CO2)(Analyze/IOCQ)]

   4 **+ 4 + 4 = 12**

5. (a) Design a sequential machine to detect the occurrence of pairs of inputs 00, 00, 11, 10, on the two inputs and give a output 1 every time the proper sequence is detected. Show the state diagram, excitation table and the steps to form the sequential circuit. [(CO2)(Analyze/HOCQ)]

   (b) What is the principle of operation and applications for the watch dog timer and a reaction timer? [(CO2)(Understand/LOCQ)]

   6 + 6 = 12

Group - D

6. (a) In the 8051 micro-controller describe the main partitions with their characteristics of the first 128 bytes of RAM that is visible to the user. [(CO3)(Remember/LOCQ)]

   (b) With the 8051 micro-controller assuming default stack area and Register 0 is selected, show the stack and stack pointer (SP) for the push and pop operations from the following instructions

   MOV R6, #27h

   MOV R1, #15h

   MOV R4, #0E9h

PUSH 6
PUSH 1
PUSH 4
POP 3
POP 2
POP 5. [(CO3)(Analyze/HOCQ)]

6 + 6 = 12

7. (a) Describe the register organization of ARM7 along with the seven processor modes (including five exception modes). [(CO4)(Remember/IOCQ)]
   (b) Using the 8051 timer mode create a square wave of 50% duty cycle (With equal portions high and low) on the P1.5 bit (Port 1 bit 5). [(CO3)(Analyze/HOCQ)]

6 + 6 = 12

Group – E

8. (a) What are limitations of uni-processor? [(CO5)(apply/IOCQ)]
   (b) How does a CMP (chip multiprocessor) resolve those issues? [(CO5)(Apply/IOCQ)]

6 + 6 = 12

9. (a) Describe a SRAM and a DRAM cell. [(CO5)(Remember/LOCQ)]
   (b) Between SRAM and a DRAM which one is used to build a cache memory and why? Which one of them is preferably used to build the main memory storage of a computer system and why? [(CO5)(Understand/LOCQ)]
   (c) Design a combinational circuit using a ROM. The circuit accepts a 3 bit number and generates an output in binary number which is square of the input number. [(CO5)(Analyse/IOCQ)]

4 + 2 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	25%	50%	25%

Course Outcome (CO):

After the completion of the course students will be able to

1. Students will be able to solve problems associated with wave propagation through anisotropic mediums.
2. Students will be able to design different components such as planar and rectangular waveguides, bends, Y- section, couplers, filters etc.
3. Students will be able to design coupled waveguides and resonators.

4. Students will be able to design photonic band-gap devices.
5. Students will understand the fabrication process for different optical devices.
6. Students will be able to characterize the basic photonic components using simple python coding

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question