DIGITAL VLSI IC DESIGN
(VLSI 5101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Value of "Lambda" in 0.18 μm Technology is
(a) 0.36 μm (b) 0.18 μm (c) 0.09 μm (d) 0.10 μm.

(ii) Pentium 4 chip belongs to below category
(a) VLSI (b) ULSI (c) GSI (d) TSI.

(iii) BDD is used in
(a) Routing (b) Logic Synthesis (c) Floorplan (d) High Level Synthesis.

(iv) For a Standard Cell Layout
(a) width is fixed (b) height is fixed
(c) none of Above (d) both height and width are fixed.

(v) LUT belongs to below one of the types of circuits
(a) CPLD (b) Gate Array (c) PLA (d) FPGA.

(vi) KL Algorithm is related to
(a) Routing (b) Logic Synthesis (c) Partitioning (d) High Level Synthesis.

(vii) With decrease of V_{DD}, the delay of an CMOS inverter
(a) decreases and then increases (b) decreases
(c) remains same (d) increases.

(viii) Minimum number of transistors required to implement CMOS logic Y = AB + CDE is:
(a) 14 (b) 12 (c) 8 (d) 10.

(ix) The output of physical design is
(a) RTL (b) circuit diagram (c) logical netlist (d) layout.

(x) 0.7 Technology Scaling enables Layout area scaling of
(a) 0.70 (b) 0.35 (c) 0.49 (d) 1.40.

Group - B

2. (a) Implement circuit of a Level-1 D-Latch using CMOS Transmission Gate (TG). [(CO1)(Evaluate/HOCQ)]
   (b) Implement circuit of a falling edge triggered D-flip flop using level-1 D-Latch and any other digital gates. [(CO1)(Evaluate/HOCQ)]
   (c) Implement circuit diagram of 2 input XNOR gate using CMOS Transmission Gate (TG). [(CO1)(Evaluate/HOCQ)]

4 + 4 + 4 = 12

3. (a) Describe Y chart. [(CO3) (Remember/LOCQ)]
   (b) Implement schematic of CMOS gate which represents function f = (ABC+D) ! (! Means Bar). [(CO2) (Apply/IOCQ)]
   (c) Evaluate stick diagram of the same CMOS gate. [(CO2) (Evaluate/HOCQ)]

4 + 4 + 4 = 12

Group - C

4. (a) What are differences between full custom design and standard cell based semi custom design ? [(CO3) (Remember/LOCQ)]
   (b) Evaluate Euler path solution of a CMOS gate which represents function f = (AB+CD) ! (! Means Bar). [(CO2) (Evaluate/HOCQ)]
   (c) Implement stick diagram of the same CMOS gate based on Euler path solution. [(CO2) (Apply/IOCQ)]

4 + 4 + 4 = 12

5. (a) Solve Euler path algorithm for the function f = (AB + C + D) ! (! Means Bar). [(CO2) (Evaluate/HOCQ)]
   (b) Implement stick diagram accordingly for the function f. [(CO2) (Evaluate/IOCQ)]
   (c) Describe difference between Behavioural and Structural model of VHDL coding using an example. [(CO4) (Analyze/IOCQ)]

4 + 4 + 4 = 12

Group - D

6. (a) Draw flow diagram of High Level Synthesis. [(CO5) (Remember/LOCQ)]
   (b) Implement BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using Ordering of a $\leq$ b $\leq$ c. [(CO5) (Evaluate/HOCQ)]
   (c) Create ROBDD diagram and corresponding optimized Boolean expression. [(CO5) (Evaluate/HOCQ)]

4 + 4 + 4 = 12

7. (a) Draw flow diagram of physical layout automation. [(CO6) (Remember/LOCQ)]
   (b) Formulate floor-planning problem with proper inputs, outputs and objective (Cost) function? [(CO6) (Evaluate/HOCQ)]

(c) Explain Lee algorithm of Maze routing. [(CO6)(Analyze/IOCQ)]

4 + 4 + 4 = 12

Group - E

8. (a) Why CMOS Transmission gate is used instead of NMOS pass transistor logic? [(CO1)(Analyze/IOCQ)]
   (b) Implement circuit of a rising edge triggered D-flip flop. [(CO1)(Apply/IOCQ)]
   (c) Implement circuit of 8 input OR gate using domino circuit. [(CO1)(Apply/IOCQ)]

4 + 4 + 4 = 12

9. (a) Draw flow diagram of physical layout automation. [(CO6)(Remember/LOCQ)]
   (b) For below channel routing problem, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG).
   Terminal connection is as follows:
   11122563040 ----- Upper Boundary
   25055330604 ----- Lower Boundary
   0 means no connection.
   Assume HV layer (V = Metal 1, H = Metal 2). [(CO6)(Apply/IOCQ)]
   (c) Provide optimum channel routing solution for above case using left edge algorithm. [(CO6)(Evaluate/HOCQ)]

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	20.83	41.66	37.5

Course Outcome (CO):

After the completion of the course students will be able to
CO1. Students will learn CMOS Circuit used in Digital VLSI Domain
CO2. Students will learn Physical Layout Design of CMOS Standard Cell
CO3. Students will learn Digital VLSI Design Methodology
CO4. Students will learn HDL coding
CO5. Students will learn EDA High Level and Logic Level Synthesis Algorithms
CO6. Students will learn EDA Physical Place and Route Automation Algorithms

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question