MICROELECTRONICS AND ANALOG VLSI DESIGN
(ECEN 4111)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) IC Chip with 1 billion transistor belongs to below category
(a) GSI (b) TSI (c) VLSI (d) ULSI.

(ii) Value of 'lambda' in 90 nm process technology node is
(a) 45 nm (b) 90 nm (c) 180 nm (d) 9 nm.

(iii) DI water is free from
(a) bacterial contamination (b) ionic contamination
(c) particulate contamination (d) all of the above.

(iv) Due to short channel effects, the threshold voltage of a MOSFET
(a) increases (b) decreases
(c) remains unaltered (d) goes to zero.

(v) Saturation region of ideal MOS transistor can be modelled as
(a) Capacitance (b) Current Source
(c) Voltage Source (d) Resistance.

(vi) Most popular scaling technique in today's nano technology is
(a) constant field scaling (b) constant voltage scaling
(c) constant energy scaling (d) constant charge scaling.

(vii) The performance of a current mirror circuit depends on
(a) channel length modulation (b) aspect ratio
(c) V_{th} (d) all of the above.

(viii) 3D transistor is created using below fabrication process
(a) SOI (b) N-Well bulk CMOS
(c) FinFET (d) Twin tub bulk CMOS.

(ix) Sputtering is a _____ process.
(a) chemical (b) physical
(c) mechanical (d) electromechanical

(x) Switched capacitor circuit realizes
(a) Capacitance (b) Resistance (c) Inductance (d) Current Source.

Group- B

2. (a) Explain Channel Length Modulation (CLM) in MOSFETs. [(CO1)(Understand/LOCQ)]
(b) Identify the appropriate region in the drain characteristics of a MOSFET that exhibits the CLM phenomenon. [(CO2)(Apply/IOCQ)]
(c) Illustrate with a suitable diagram, how the capacitance of a MOSFET varies with the applied gate voltage. [(CO1)(Analyze/IOCQ)]
3 + 5 + 4 = 12

3. (a) What is constant field scaling of MOSFETs? [(CO2)(Remember/LOCQ)]
(b) Show the effects of constant field scaling on the packing density and power dissipation density of MOSFETs. [(CO2)(Apply/IOCQ)]
(c) For a 0.8 μm process technology for which t_{ox}=15 nm and μ_n=550 cm^2 /Vs. Calculate C_{ox}, k_n' and the overdrive voltage required to operate the transistor (with aspect ratio to be 10) in the saturation region with I_d= 0.2 mA. Determine the minimum value of V_{ds} needed. [(CO2)(Evaluate/HOCQ)]
2 + 5 + 5 = 12

Group - C

4. (a) Mention the uses of SiO_2 in the semiconductor fabrication industry. [(CO3)(Remember/LOCQ)]
(b) Differentiate between wet and dry oxidation. [(CO3)(Understand/LOCQ)]
(c) Prove that if a SiO_2 layer is grown by thermal oxidation, the thickness of Silicon consumed is 0.44 times the thickness of SiO_2. Given, the molecular weight of Si is 28.9 g/mol and the density of Si is 2.33 g/cc. The corresponding values for SiO_2 are 60.08 /mol and 2.21g/cc. [(CO3)(Evaluate/HOCQ)]
2 + 4 + 6 = 12

5. (a) Explain CMOS Fabrication flow step by step using self aligned N-Well process techniques. [(CO3)(Analyze/IOCQ)]
(b) Explain common centroid layout using an example. [(CO3)(Analyze/IOCQ)]
(c) Explain Structure of FinFET transistor. [(CO3)(Analyze/IOCQ)]
6 + 3 + 3 = 12

Group - D

6. (a) Draw a flow chart to illustrate the steps of analog VLSI circuit design. [(CO4)(Remember/LOCQ)]
(b) Compare the large signal models of an ideal and a practical MOSFET at low frequencies. [(CO4)(Analyze/IOCQ)]
(c) Derive an expression to show the dependence of the transconductance on the aspect ratio of a MOSFET. [(CO4)(Create/HOCQ)]
4 + 5 + 3 = 12

7. (a) Draw small signal high frequency model for NMOS and explain. [(CO4)(Analyze/IOCQ)]
   (b) Evaluate how diode AC resistance is dependent on NMOS transconductance when the NMOS is used as diode? [(CO4)(Evaluate/HOCQ)]
   (c) Evaluate how $V_{DD}/2$ can be realized using NMOS based Supply Voltage (V_{DD}) Divider Circuit. [(CO4)(Evaluate/HOCQ)]

4 + 4 + 4 = 12

Group - E

8. (a) Evaluate how basic current mirror circuit can be designed as current multiplier where $I_{out}/I_{in} = 6$. [(CO4)(Evaluate/HOCQ)]
   (b) Explain CMOS bandgap reference circuit. [(CO4)(Analyse/IOCQ)]
   (c) Evaluate how cascode current sink can increase output resistance. [(CO4)(Evaluate/HOCQ)]

4 + 4 + 4 = 12

9. (a) Explain level shifter circuit of GPIO transmitter (Level Up). [(CO6)(Analyse/IOCQ)]
   (b) Explain circuit of switched capacitor integrator. [(CO6)(Analyse/IOCQ)]
   (c) Evaluate differential gain of MOS based differential amplifier with load resistance, R_D and transconductance gain, g_m of MOS transistors as used as differential pair. [(CO5)(Evaluate/HOCQ)]

2 + 4 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	15.62	46.87	37.5

Course Outcome (CO):

After the completion of the course students will be able to

1. Understand the fundamentals of MOSFET Device Physics.
2. Correlate the fundamental understanding with the evolving VLSI Design Trends and Challenges.
3. Understand the IC Fabrication Process Flow leading to the practical realization of the scaled MOSFETs.
4. Analyze MOS-based analog VLSI sub-circuits and design them namely, current mirrors, voltage, and current references.
5. Design MOS circuits of practical importance e.g., common-source amplifiers and differential amplifiers.
6. Understand and apply the knowledge of analog sampled data circuits to synthesize practical circuits such as switched- capacitor filters.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question