MICROPROCESSORS AND MICROCONTROLLERS
(ECEN 3104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Which of the following is the correct option for an 8085 microprocessor?
(a) 8-bit data bus and 16-bit address bus
(b) 8-bit data bus and 8-bit address bus
(c) 16-bit data bus and 8-bit address bus
(d) 16-bit data bus and 16-bit address bus.

(ii) The instructions INR and DCR affects all the flags except the
(a) Carry flag (b) Sign flag (c) Parity flag (d) Auxiliary Carry flag.

(iii) In 8085 microprocessor, which signal is used to insert WAIT?
(a) READY (b) ALE (c) HOLD (d) INTR.

(iv) The bits of the PSW Register which are responsible for selection of register banks of 8051 are
(a) PSW.3 and PSW.4 (b) PSW.3 and PSW.2
(c) PSW.3 and PSW.1 (d) PSW.3 and PSW.5.

(v) XCHG instruction of 8085 exchanges the content among which register pairs?
(a) Top of the stack with contents of register pair
(b) BC and DE register pairs
(c) HL and DE register pairs
(d) None of the above.

(vi) PUSH and POP operations are performed by which of the following options?
(a) PC register (b) General purpose registers
(c) SP register (d) Link register.

(vii) In an 8085 microprocessor, the contents of the accumulator and the carry flag are A7 (in hex) and 0, respectively. If the instruction RLC is executed, then the contents of the accumulator (in hex) and the carry flag, respectively will be which of the following option?
(a) 4E and 0 (b) 4E and 1 (c) 4F and 0 (d) 4F and 1.

(viii) The BIU pre-fetches the instruction from memory and store them in which of the following?
(a) Queue (b) Register (c) Memory (d) Stack.

(ix) How many bytes of bit addressable memory are present in 8051 based microcontrollers?
(a) 8 bytes (b) 32 bytes (c) 16 bytes (d) 128 bytes.

(x) How many address lines will be required for an 8-K byte (1024 x 8 = 8192 registers) memory chip?
(a) 10 (b) 11 (c) 12 (d) 13.

Group - B

2. (a) Write two examples of branching operations of an 8085 instruction set?
[(CO1)(Apply/IOCQ)]

(b) Assume that 82 (in hex) and 96 (in hex) data are manually stored in 9000H and 9001H respectively in an 8085 microprocessor. Check and evaluate the sign flag, zero flag, parity flag and carry flag after addition of these two above data.
[(CO1)(Evaluate/HOCQ)]

(c) Given the following instructions of an 8085 microprocessor, identify the instruction word size (byte) and explain its function.
(i) ADI 59H (ii) LDA 2050H. [(CO1)(Remember, Understand/LOCQ)]

3 + 5 + (2 + 2) = 12

3. (a) Write instructions to load the 16-bit number 2050H in the register pair HL using LXI and MVI opcodes and explain the difference between the two instructions.
[(CO1)(Analyse/IOCQ)]

(b) Identify the addressing modes of the following instructions:
(i) MOVA, B (ii) ORI 48H (iii) CMA (iv) LDAX D (v) LDA 2080H.
[(CO2)(Analyse/IOCQ)]

(c) Write two examples each for immediate addressing modes and implicit addressing modes? [(CO2)(Understand, Apply/LOCQ,IOCQ)]

4 + 5 + 3 = 12

Group - C

4. (a) The memory address of the last location of an 1K byte (1024) byte memory chip is given as FBFF (in hex). Specify the starting address and the no. of pages in the chip?
[(CO2)(Analyze, Evaluate/IOCQ, HOCQ)]

(b) Two machine codes 3EH and 32H (MVI A, 32H) are stored in memory location 4000H and 4001H respectively. With the help of timing diagram calculate the time required to execute the entire instruction cycle if the clock frequency is 2MHz.
[(CO2)(Evaluate/HOCQ)]

(c) What are instruction cycle, machine cycle and T-states of an 8085 microprocessor?
[(CO2)(Remember/LOCQ)]

4 + (2 + 3) + 3 = 12

5. (a) Design an ALP along with a flow chart to generate a Fibonacci series generating sixteen numbers. Write the output in Hex code along with corresponding memory locations where the numbers will be stored. [(CO3)(Design/HOCQ)]
   (b) Describe the register section of 8086. [(CO4)(Remember/LOCQ)]
   8 + 4 = 12

Group - D

6. (a) Draw the block diagram of 8259A. [(CO5)(Remember/LOCQ)]
   (b) Differentiate between priority modes that are available under software control in the 8259A? [(CO5)(Analyse/IOCQ)]
   (c) What are the tasks that are performed by 8259A? [(CO5)(Remember/LOCQ)]
   3 + 3 + 6 = 12

7. (a) Describe the control logic section of 8255A? Mention some application of this programmable peripheral interface? [(CO5)(Remember/LOCQ)]
   (b) What is meant by BSR mode? Design a BSR control word subroutine to set bits PC_7 and PC_3 and reset them after 10ms. Consider that a delay subroutine is available and address of control register is 83H. [(CO5)(Design/HOCQ)]
   (4 + 2) + (2 + 4) = 12

Group - E

8. (a) Define the unconditional jumps present in 8051? [(CO6)(Remember/LOCQ)]
   (b) Illustrate in details about different addressing modes of 8051? [(CO6)(Apply/IOCQ)]
   (c) Write a program to copy the value 55 (in hex) into RAM memory locations 40 (in hex) to 45 (in hex) using direct addressing mode in 8051? [(CO6)(Evaluate,Create/HOCQ)]
   3 + 6 + 3 = 12

9. (a) Differentiate between a microprocessor and microcontroller with proper block diagram. [(CO6)(Analyse/IOCQ)]
   (b) Analyse the differences between polling and interrupt with respect to 8051 microcontroller. [(CO6)(Analyse/IOCQ)]
   (c) Describe the indexed addressing modes of 8051 controller with example. [(CO6)(Remember/LOCQ)]
   4 + 5 + 3 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	36.46	31.25	32.29

Course Outcomes (CO):

After the completion of the course students will be able to

1. Demonstrate the knowledge of Digital Electronics with learning of the microprocessor and microcontroller.
2. Develop the concepts of CPU, timing and control signals I/O devices, and various BUS structure.
3. Learn about interrupts, stack and subroutine and write ALPs for given problems with flowcharts.
4. Conceptualize the architecture of 8086 family & ARM basics along with its parallel application.
5. Understand interfacing of processor with memory and I/O devices and analyze their problems.
6. Analyze microcontroller 8051 architecture in terms of Ports, Memory, Counters and Timers.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.