ANALOG & DIGITAL ELECTRONICS
(ELEC 2102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Which of the following oscillators uses one inductor and two capacitors in the feedback circuit?
(a) Hartley oscillator (b) Colpitts oscillator
(c) Wien bridge oscillator (d) Phase shift oscillator.

(ii) To avoid false triggering, the RESET pin of 555 timer is generally connected to
(a) Threshold (b) +Vcc (c) Ground (d) Trigger.

(iii) The two input terminals of an ideal Op amp are at the same potential because
(a) the two input terminals are directly shorted to ground
(b) the input impedance of the Op amp is infinity
(c) the output impedance of the Op amp is zero
(d) the open loop gain of the Op amp is infinity.

(iv) A zero crossing detector circuit generates
(a) triangular waveform (b) sinusoidal waveform
(c) sawtooth waveform (d) square waveform.

(v) The fundamental frequency of a crystal oscillator is
(a) directly proportional to the thickness of the crystal
(b) inversely proportional to the thickness of the crystal
(c) independent of the thickness of the crystal
(d) proportional to the temperature of the crystal.

(vi) When a Boolean expression contains four variables, the number of cells in Karnaugh map must be
(a) $2^4 + 1$ (b) $2^4 - 1$ (c) 2^4 (d) 2^3.

(vii) Minimum number of NAND gates required to realize an XNOR gate is
(a) 3 (b) 2 (c) 5 (d) 4.

(viii) The number of select lines required in a single input n-output (1:n) demultiplexer is
(a) 2 (b) n (c) $\log_2 n$ (d) 2n.

(ix) Number of 2:1 multiplexers required to construct an 8:1 multiplexer is
(a) 5 (b) 6 (c) 7 (d) 8.

(x) Which of the following states is not allowed for an S-R flip flop
(a) S=0; R=0 (b) S=1; R=0 (c) S=1; R=1 (d) S=0; R=1.

Group- B

2. (a) Calculate the values of I, I_Z and I_L for the circuit shown in Fig.1. It is given that breakdown voltage of the zener diode is 5V, R = 1.5 kΩ and R_L = 1kΩ.
[(CO1) (Analyze/IOCQ)]

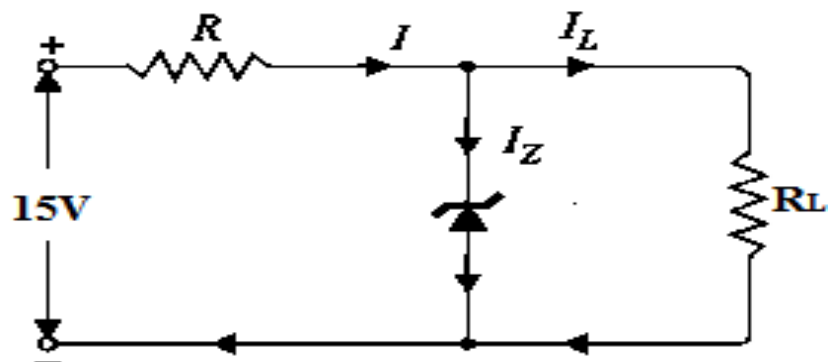

Fig.1

(b) Design a non-inverting adder circuit to obtain an output voltage V_o such that $V_o = V_a + 2V_b$
where V_a and V_b are the input voltages. [(CO2) (Create/HOCQ)]

(c) In the circuit shown in Fig.2 the Silicon transistor has β = 75 and collector voltage V_c = 9V. Determine the ratio of R_B and R_c.
[(CO1) (Analyze/IOCQ)]

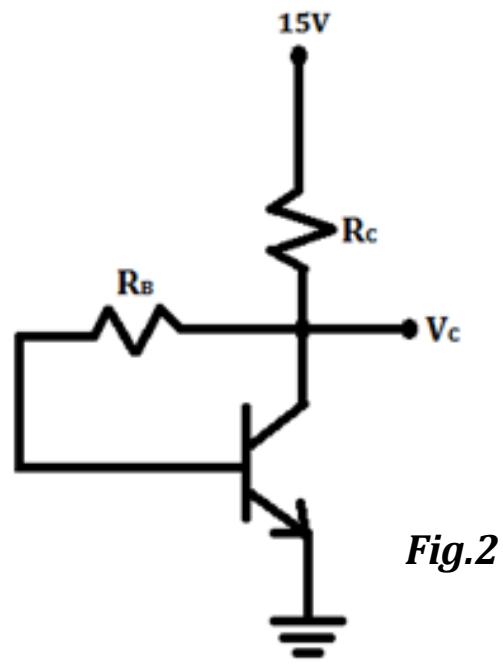

Fig.2

4 + 4 + 4 = 12

3. (a) Model the linear differential equation using minimum number of operational amplifiers: $2\frac{d^2y}{dt^2} + 2\frac{dy}{dt} + y = 5$ [(CO1) (Apply/IOCQ)]

(b) Calculate R_1 / R_2 and V_R if the Schmitt trigger circuit of Fig.3 uses 6V Zener diodes with V_D = 0.7 V. Consider the upper threshold voltage, V_{UTP} = 0 and the hysteresis voltage, V_H = 0.2V.
[(CO2)(Apply/IOCQ)]

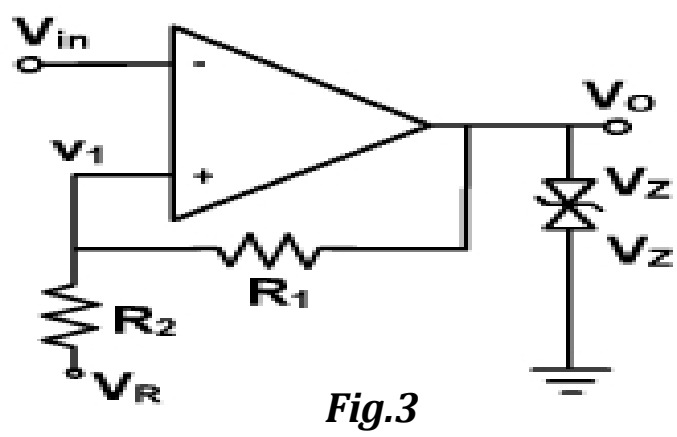

Fig.3

(c) Derive the expression of closed loop gain for a voltage series feedback amplifier. [(CO2)(Apply/IOCQ)]

(d) Define slew rate. [(CO1)(Remember/LOCQ)]

5 + 3 + 3 + 1 = 12

Group - C

4. (a) Derive the expression of oscillation frequency for RC phase shift oscillator using an operational amplifier. [(CO3) (Apply/IOCQ)]

(b) Design a triangular wave generator with oscillation frequency f_o = 1.5kHz and output voltage v_o(p-p) = 5V. Consider supply voltages = ±15V. [(CO3) (Create/HOCQ)]

9 + 3 = 12

5. (a) Explain the working principle of a monostable multivibrator circuit using 555 timer. Draw the trigger, output and capacitor voltage waveforms. Derive the expression of the timing period. [(CO3)(Apply/IOCQ)]

(b) Design a voltage controlled oscillator circuit with nominal frequency, f_o = 25kHz for a control voltage V_C = 6V. Consider supply voltage of IC566 VCO = 12V. [(CO3)(Create/HOCQ)]

(c) State Barkhausen criteria. [(CO3)(Remember/LOCQ)]

8 + 2 + 2 = 12

Group – D

6. (a) Subtract $(10110)_2$ from $(11011)_2$ using 2's complement method. Subtract also using direct method and compare both results. [(CO4) (Understanding/LOCQ)]

(b) Apply the knowledge of K map to simplify the following Boolean function and implement it using suitable logic gates:
$F(A,B,C,D) = \sum_m (0,1,2,4,5,12,13,14) + \sum_d (6,8,9)$. [(CO4) (Apply/IOCQ)]

(c) Determine the canonical POS form of the function Y=A+BC. [(CO4) (Create/HOCQ)]

4 + 5 + 3 = 12

7. (a) Discuss briefly about binary to octal (3:8) decoder. [(CO5)(Understanding /LOCQ)]

(b) Illustrate the design of a 5:32 line decoder using 3:8 line decoders with active high enable input and 2:4 decoder. Use block diagram of the components. [(CO5)(Apply/IOCQ)]

(c) Design a 3 bit even parity generator circuit using NAND gate only. [(CO5)(Create/IOCQ)]

4 + 5 + 3 = 12

Group - E

8. (a) Describe the working of an SR latch using NOR gates. [(CO6)(Remember/LOCQ)]

(b) Construct a T flip-flop using S-R flip-flop. [(CO6)(Apply/IOCQ)]

(c) Develop the characteristic equation of D flip flop. [(CO6)(Create/HOCQ)]

4 + 5 + 3 = 12

9. (a) Explain the working of a 4 bit SISO shift register for right shift mode.
[(CO6)(Remember/LOCQ)]

(b) Design a MOD 6 synchronous up counter and explain its working principle.
[(CO6)(Create/HOCQ)]

4 + 8 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	19.78	56.25	23.97

Course Outcome (CO):

After the completion of the course students will be able to

- Recall basic principles of diodes, transistors and OPAMPs.
- Understand basic principles of OPAMP based circuits for linear and nonlinear operations and analyze their implications.
- Acquire knowledge about different waveform generators, 555 timers, ADCs and DACs and their applications.
- Recall number systems and Boolean algebra.
- Understand Boolean algebra based realisation of logic gates and design of various arithmetic and combinational circuits.
- Design and analyze various sequential circuits like synchronous and asynchronous counters, shift registers using flip flops.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question