# DIGITAL SYSTEMS DESIGN
## (ECEN 2002)

**Time Allotted : 3 hrs** **Full Marks : 70**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

## Group – A
### (Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The equivalent hexadecimal number of the octal number $(7642.675)_8$ is
(a) (12AB.ABC)H (b) $(324C.CAB)_H$ (c) $(54.FF)_H$ (d) $(FA2.DE8)_H$

(ii) How many full-adders are required to construct an m-bit parallel adder?
(a) m/2 (b) m-1 (c) m (d) m+1.

(iii) 2's complement of a four bit binary number 1101 is _____ .
(a)1011 (b)1111 (c)0011 (d)1110

(iv) How many Flip-Flops are required for a Mod–13 Counter ?
(a) 5 (b) 6 (c) 3 (d) 4.

(v) The Digital Logic Family which has the lowest power dissipation is
(a) ECL (b) TTL (c) CMOS (d) PMOS.

(vi) The number of select lines required in a single input and 256 output DEMUX is
(a) 8 (c) 32 (b) 16 (d) 64.

(vii) In a JK flip flop, $Q_{i-1} = 1$, $Q_{i-1}' = 0$, for J = K = CLK = 1, $Q_i$ = ___, $Q_i'$ = _____
(a) $Q_i = 0, Q_i' = 1$ (b) $Q_i = 1, Q_i' = 0$ (c) $Q_i = 0, Q_i' = 0$ (d) $Q_i = 1, Q_i' = 1$

(viii) In a Demultiplexer of general configuration, there are ___ input terminals, _ output terminals and __ selector terminals.
(a) n, 1, $2^n$ (b) 1, $2^n$, n (c) $2^n$, n, 1 (d) n, $2^n$, 1

(ix) Which is the fastest logic family?
(a) ECL (b) DTL (c) TTL (d) RTL.

(x) Which of the memory is a volatile memory?
(a) ROM (b) RAM (c) PROM (d) EEPROM.

## Group- B

2. (a) Perform the following arithmetic operations:
(i) $(25 - 13)_{10}$ in binary form by 1's compliment method

(ii) $(16 - 26)_{10}$ in binary form by 2's compliment method.
[(CO1)(Understand/LOCQ)]

(b) State the following:
(i) De Morgan's Theorem
(ii) Commutative Law
(iii) Associative Law
(iv) Distributive Law
(v) Identity Law
(vi) Idempotent Law
(vii) Annulment Law
(viii) Absorptive Law. [(CO1)(Remember/LOCQ)]

(c) Implement the following:
(i) AND gate by NOR gate
(ii) NOR gate by NAND gate
(iii) XOR gate by NOR gate. [(CO1)(Understand/LOCQ)]

**4 + 4 + 4 = 12**

3. (a) Convert the following binary number into gray code and vice versa
(i) $(110001110)_2=(?)_{GRAY}$ (ii) $(11111000011)_{GRAY}=(?)_2$. [(CO2)(Remember/LOCQ)]
(b) Design a combinational circuit that accepts a 3-bit number as input and generates an output binary number equal to square of the input number. [(CO2)(Analyse/IOCQ)]

**4 + 8 = 12**

## Group - C

4. (a) Implement a Full Adder-cum-Full Subtractor circuit by utilizing 2:1 Mulptiplexer.
[(CO2)(Create/HOCQ)]
(b) Show with proper and sufficient sketch how can 2:4 Decoder be converted to 1:4 Demultiplexer. [(CO2)(Analyze/IOCQ)]
(c) Implement a Full Subtractor circuit by 3:8 Decoder. [(CO2)(Create/HOCQ)]

**5 + 2 + 5 = 12**

5. (a) Design a 5 bit register using D flip flops. [(CO3)(Analyse/IOCQ)]
(b) Design a MOD-5 synchronous counter with any flip flop of your choice.
[(CO3)(Evaluate/HOCQ)]

**6 + 6 = 12**

## Group - D

6. (a) Explain the advantage of D and JK flip flops in comparison to SR flip flop and advantage of JK flip flop in comparison to D flip flop. [(CO3)(Understand/LOCQ)]
(b) Convert SR flip flop to:- (i) D flip flop, (ii) JK flip flop. [(CO3)(Analyze/IOCQ)]
(c) State the differences between combinational logic circuit and sequential logic circuit.
[(CO2, CO3)(Remember/LOCQ)]
(d) What is race around condition? How is it eliminated? [(CO3)(Understand/LOCQ)]

**2 + 4 + 3 + 3 = 12**

7. (a) A flip flop has a 10ns delay from the time its CLK goes from 1 to 0 to the time its output is complemented. What is the maximum delay in a 10 bit binary ripple counter that uses these flip flops? What is the maximum frequency at which the counter can operate reliably? [(CO3)(Evaluate/HOCQ)]
   (b) Draw the waveforms of a 4 bit binary ripple UP counter. [(CO3)(Analyse/IOCQ)]
   (c) Draw and explain the operation of a 4 bit parallel in serial out shift register. [(CO3)(Analyse/IOCQ)]

**4 + 4 + 4 = 12**

## Group - E

8. (a) Explain the circuit diagram and operation of 4 bit BCD adder. [(CO2)(Remember/LOCQ)]
   (b) A 10-bit DAC provides an analog output which has a maximum value of 10.23 volts. What is the resolution of the DAC ? [(CO4)(Evaluate/HOCQ)]

**9 + 3 = 12**

9. (a) Implement the function Y = F (A, B, C) = (A + B).(B + C).(C + A) by CMOS logic. [(CO5)(Create/HOCQ)]
   (b) Describe the logic operation of 2 input TTL NAND gate. [(CO5)(Apply/IOCQ)]

**8 + 4 = 12**

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| Cognition Level | LOCQ | IOCQ | HOCQ |
|---|---|---|---|
| Percentage distribution | 34.37 | 33.33 | 32.3 |

**Course Outcome (CO):**

After the completion of the course students will be able to

1. Make use of the concept of Boolean algebra to minimize logic expressions by the algebraic method, K-map method, and Tabular method.
2. Construct different Combinational circuits like Adder, Subtractor, Multiplexer, De-Multiplexer, Decoder, Encoder, etc.
3. Design various types of Registers and Counters Circuits using Flip-Flops (Synchronous, Asynchronous, Irregular, Cascaded, Ring, Johnson).
4. Outline the concept of different types of A/D and D/A conversion techniques.
5. Realize basic gates using RTL, DTL, TTL, ECL, and CMOS logic families.
6. Relate the concept of Flip flops to analyze different memory systems including RAM, ROM, EPROM, EEROM, etc.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question