COMPUTER ORGANISATION AND ARCHITECTURE
(INFO 2111)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) How many address bit is required for 1024 × 8 memory chip?
(a) 1024 (b) 5 (c) 10 (d) 12.

(ii) The minimum number of operands with any instruction is
(a) 1 (b) 0 (c) 2 (d) 3.

(iii) The BOOT sector files of the system are stored in ____
(a) Harddisk (b) ROM (c) RAM (d) Motherboard.

(iv) Cache memory is made upon
(a) Bipolar Semiconductor (b) Unipolar semiconductor device
(c) Optical disk (d) Magnetic storage.

(v) The basic principle of Von-Neumann computer is
(a) storing program and data in separate memory
(b) storing program and data in same memory
(c) using pipeline architecture
(d) none of these.

(vi) What is the default value of accumulator in booth's multiplication of two 4-bit binary numbers?
(a) 0 (b) 1 (c) 0000 (d) 00000.

(vii) Systolic array is an example of _____ architecture.
(a) MIMD (b) MISD (c) SIMD (d) SISD

(viii) The situation wherein the data of operands are not available is called _____.
(a) Data hazard (b) Stock (c) Deadlock (d) Structural hazard

(ix) The periods of time when the unit is idle is called as ____
(a) Stalls (b) Bubbles
(c) Hazards (d) Both Stalls and Bubbles.

(x) In super-scalar processors, _____ mode of execution is used.
(a) In-order (b) Post order
(c) Out of order (d) none of the mentioned

Group- B

2. (a) Describe Von-Neumann bottleneck and its solution. [(CO1)(Understand/LOCQ)]
(b) Final carry in Carry Look Ahead Adder is not dependent on intermediate step's carry- Justify. [(CO2)(Evaluate/HOCQ)]
(c) Evaluate 17 by 4 with the help of non restoring division algorithm. [(CO2)(Evaluate/HOCQ)]
(2 + 2) + 4 + 4 = 12

3. (a) Evaluate -12 X -7 using Booth's multiplication algorithm. [(CO2)(Evaluate/HOCQ)]
(b) Construct Zero and two and instruction set for the following instruction.
((A+B)/D) *E [(CO1)(Create/HOCQ)]
7 + 5 = 12

Group – C

4. (a) Consider the cache has 4 blocks. For the memory references-
5, 12, 13, 17, 4, 12, 13, 17, 2, 13, 19, 13, 43, 61, 19
Evaluate the hit ratio for the following.
FIFO, LRU, Direct mapping. [(CO4)(Evaluate/HOCQ)]
(b) Briefly explain Set Associative mapping. [(CO3)(Understand/LOCQ)]
(c) Define write back and write through policies in cache memory? [(CO3)(Remember/LOCQ)]
6 + 4 + 2 = 12

5. (a) A computer has a main memory of 64K×16 and cache memory of 1K words. The cache uses direct mapping with a block size of four words.
Solve the following:
(i) How many bits are there in the TAG, INDEX, and word fields of the address format?
(ii) How many bits are there in each word of cache?
(iii) How many blocks can the cache accommodate? [(CO3)(Apply/IOCQ)]
(b) Describe Handshaking protocol in the context of input output unit. [(CO4)(Understand/LOCQ)]
9 + 3 = 12

Group – D

6. (a) Consider the five- stage pipelined processor specified by the following reservation table.

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

Solve the following:

(i) List the set of forbidden latencies and the collision vector.

(ii) Draw a state transition diagram showing all possible initial sequences (cycles) without causing a collision in the pipeline.

(iii) List all the simple cycles from the state diagram.

(iv) Identify the greedy cycles among the simple cycles.

(v) What is the minimum average latency (MAL) of this pipeline?

[(CO5)(Apply/IOCQ)]

(2 + 4 + 2 + 2 + 2) = 12

7. (a) Derive and discuss the speed up formula of Pipeline. When the maximum speed up is achieved? [(CO5)(Understand/LOCQ)]

(b) Consider the execution of an object code with 2×10^6 instructions on a 400 MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles[CPI] needed for each instruction type are given below based on the result of a program trace experiment:

Instruction Type	CPI	Instruction Mix
Arithmetic & Logic	1	60%
Load /Store with cache hit	2	18%
Branch	4	12%
Memory Reference with cache miss	8	10%

Solve the following:

(i) Calculate the average CPl when the program is executed on a uni-processor with the above trace results.

(ii) Calculate the corresponding MIPS rate based on the CPI obtained in part.

[(CO5)(Apply/IOCQ)]

(3 + 3) + 6 = 12

Group - E

8. (a) Describe the Omega, Baseline and Crossbar interconnection network with diagram. [(CO6)(Understand/LOCQ)]

(b) State the factors which affect the performance of an interconnection network.

[(CO6) (Analyze/IOCQ)]

3 + (3 + 3 + 3) = 12

9. (a) Describe Flynn's Taxonomy? Explain two of them with block diagram. [(CO6)(Understand/LOCQ)]

(b) Discuss in detail the hardwired control unit. [(CO6)(Understand/LOCQ)]

(2 + 4) + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	36.17	38.29	25.53

Course Outcome (CO):

After the completion of the course students will be able to

1. Understand the instruction formats and addressing modes in the context of computer architecture.
2. Design the ALU for different arithmetical and logical problems and apply the knowledge of different multiplication and division algorithm.
3. Understand the memory hierarchy (Register, Cache, Primary and Secondary).
4. Analyze different memory technologies and related replacement techniques.
5. Analyze the types of pipeline including instruction pipeline and arithmetic pipeline.
6. Understand different types of Multiprocessor architectures and types of Control Units.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question