# ELECTRONIC DESIGN AUTOMATION
## (ECEN 3106)

**Time Allotted : 3 hrs** **Full Marks : 70**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

## Group – A
### (Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Value of "Lambda" in 180 nm technology is
(a) 180 nm (b) 90 nm (c) 360 nm (d) 100 nm.

(ii) PMOS transistor switch passes
(a) weak "zero" (b) strong "zero" (c) strong "one" (d) both (a) & (c).

(iii) Most popular interconnect material is
(a) Gold (b) Silver (c) Aluminium (d) Silicon Dioxide.

(iv) For a standard cell layout
(a) width is fixed (b) height is fixed
(c) both height and width are fixed (d) none of above.

(v) Characterization categories of each cell in standard cell based design include
(a) circuit simulation model (b) timing simulation model
(c) fault simulation model (d) all of the above.

(vi) NMOS Transistor in linear region can be modelled as
(a) open circuit (b) current source
(c) resistance (d) voltage source.

(vii) Detailed routing includes
(a) switchbox routing (b) channel routing
(c) both (a) & (b) (d) none of the above.

(viii) The output of physical design is
(a) circuit diagram (b) logical netlist (c) layout (d) RTL.

(ix) The full form of RTL is
(a) Random Transfer Level (b) Register Transistor Level
(c) Regular Transistor Level (d) Register Transfer Level.

(x) Logic optimized representation of Boolean function is given by
(a) BDD (b) ROBDD (c) terminal node (d) non-terminal node.

## Group - B

2. (a) Define the input-to-output signal propagation delay times of a single stage CMOS inverter circuit with graphical illustration. [(CO2)(Remember/LOCQ)]
   (b) Briefly explain the concept of noise immunity and noise margin. [(CO2)(Understand/LOCQ)]
   (c) Evaluate the logic function *F* from the circuit in Fig.1. Design a circuit to implement the same logic function *F* using NOR gates. [(CO2)(Create/HOCQ)]

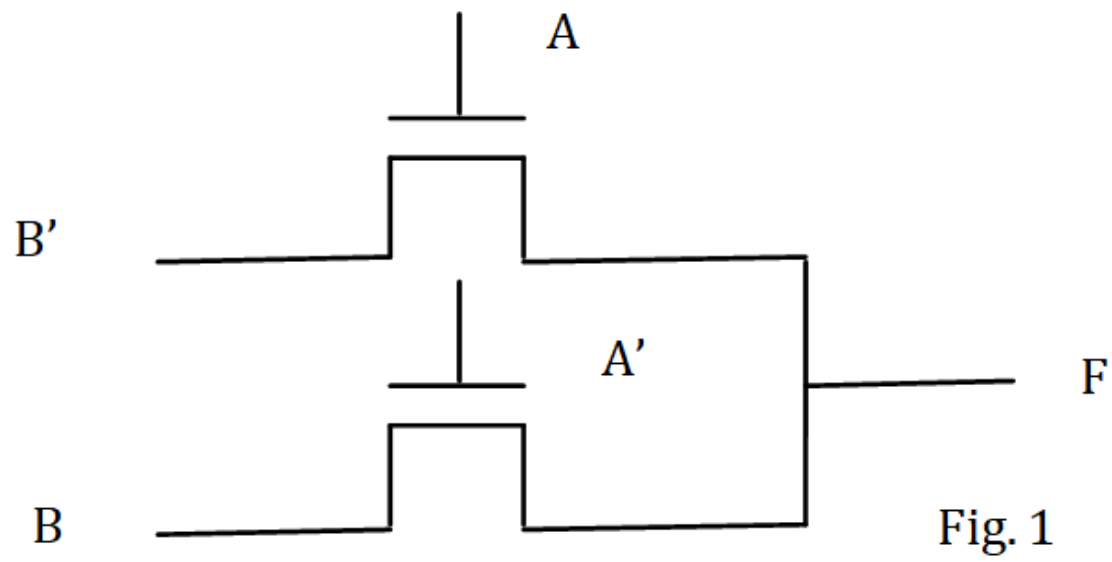


Fig. 1

**4 + 3 + 5 = 12**

3. (a) Explain the differences between full custom design and std cell based semi custom design. [(CO1)(Analyze/IOCQ)]
   (b) Implement schematic of CMOS gate which represents function f = (A+BC) ! (! Means Bar). [(CO2)(Analyse/IOCQ)]
   (c) Evaluate Stick diagram of the same CMOS gate. [(CO2)(Evaluate/HOCQ)]

**4 + 4 + 4 = 12**

## Group - C

4. (a) Explain the concept of process node and Leff with proper diagram. [(CO1)(Understand/LOCQ)]
   (b) Distinguish between PLA and PAL? [(CO1)(Understand/LOCQ)]
   (c) A large-scale fast prototyping system has been produced by using FPGAs. Outline the features and weaknesses of such prototyping systems for proof of design concepts and verification in view of effort and speed performance of the design. [(CO1)(Apply/IOCQ)]

**3 + 3 + 6 = 12**

5. (a) Solve Euler path algorithm for the function f =(AB + CD) ! (! Means Bar). [(CO2)(Evaluate/HOCQ)]
   (b) Evaluate Stick diagram accordingly [(CO2)(Evaluate/HOCQ)]
   (c) Describe difference between behavioural and dataflow model of Verilog coding using an example. [(CO5)(Analyze/IOCQ)]

**4 + 6 + 2 = 12**

## Group - D

6. (a) Draw the flowchart showing VLSI design cycle and identify the blocks corresponding to front end and back end design. [(CO4)(Understand/LOCQ)]
   (b) Briefly explain RTL synthesis (logic synthesis). [(CO4)(Understand/LOCQ)]
   (c) Implement the design of 4:1 MUX using two 2:1 MUX using Verilog code and mention the name of this modelling style. [(CO6)(Apply/IOCQ)]

**4 + 2 + 6 = 12**

7. (a) Define *BDD* with its features with graphical illustration. [(CO5) (Understand /LOCQ)]
   (b) Draw the *BDD* for *XNOR* function. [(CO5) (Apply/LOCQ)]
   (c) Explain the concept of graph covering in context of technology mapping (library mapping). Apply this concept to cover the graph shown in Fig. 2 in two possible methods and then justify which one is the optimal covering. [(CO5)( Apply/IOCQ)]

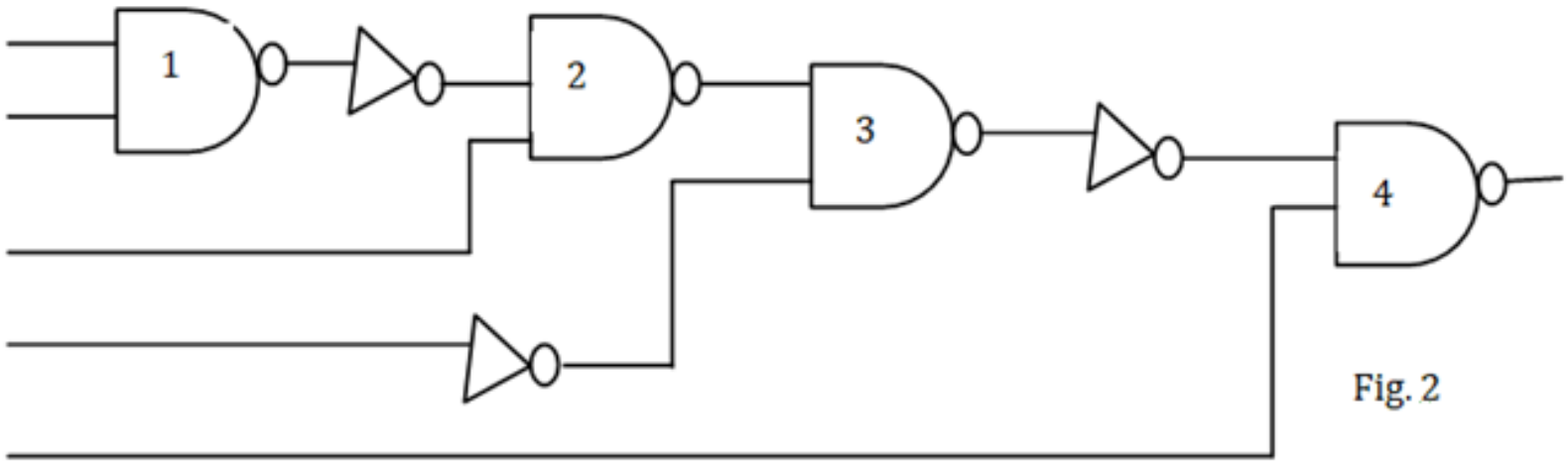


Fig. 2

**3 + 3 + 6 = 12**

## Group – E

8. (a) Briefly discuss the different steps in physical design with proper flowchart. [(CO6)(Understand/LOCQ)]
   (b) Consider Fig. 3 with initial partition *S1 = {C, D, E, F}* and *S2 = {A, B, G, H}.* Determine cut size. If you do the node swapping of (*B, D*), compute the new cut size applying *K-L* partitioning algorithm. [(CO6)(Evaluate/HOCQ)]

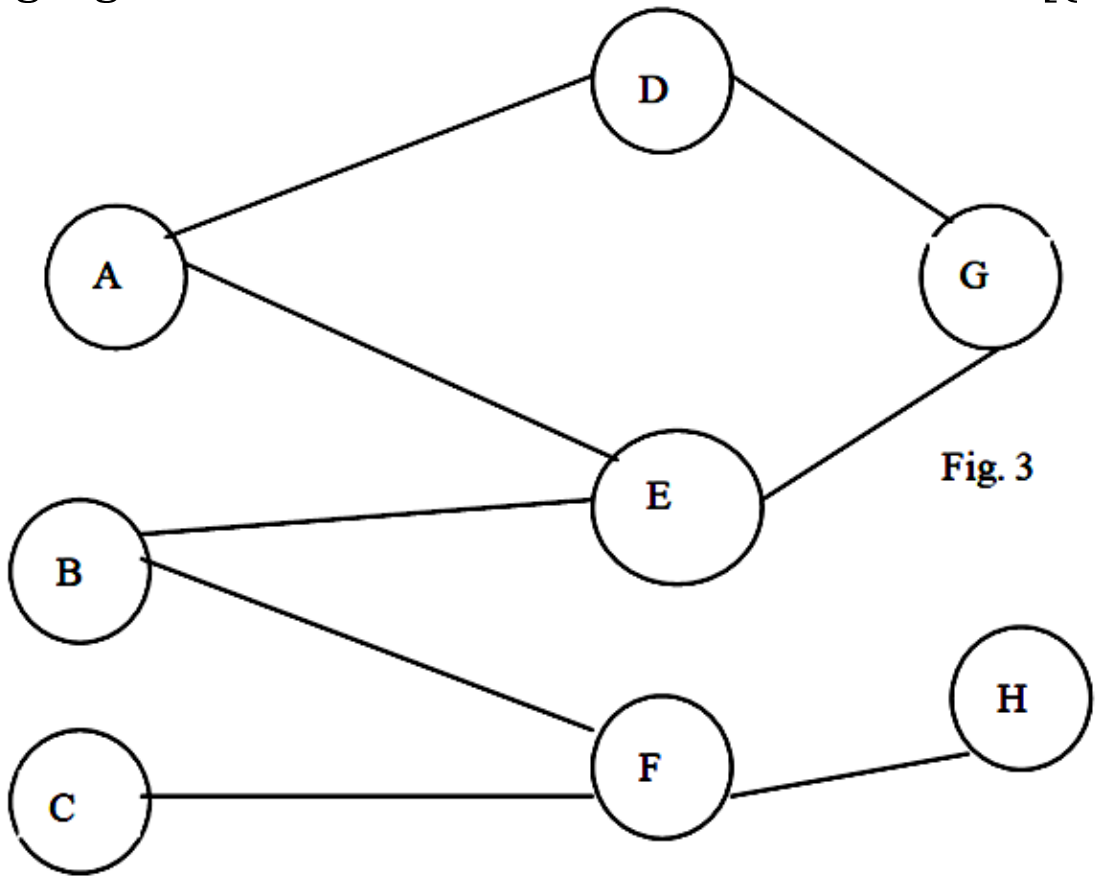


Fig. 3

**6 + 6 = 12**

9. (a) For below channel routing problem, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG)
Terminal Connection is as follows:
11122563040 ----- Upper Boundary
25055330604 ----- Lower Boundary
0 means no Connection.
Assume HV Layer (V = Metal 1, H = Metal 2) [(CO6)(Analyze/IOCQ)]

(b) Evaluate optimum channel routing solution for above case using left edge algorithm. [(CO6)(Evaluate/HOCQ)]

(c) Write problem formulation of global routing using Steiner tree. [(CO6)(Analyze/IOCQ)]

**4 + 4 + 4 = 12**

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| Cognition Level | LOCQ | IOCQ | HOCQ |
|---|---|---|---|
| Percentage distribution | 32.30 | 42.70 | 25 |

**Course Outcome (CO):**

After the completion of the course students will be able to

CO.1. Getting exposure to VLSI Design Cycle, Process nodes and Design Challenges.
CO.2. Designing of Industry Standard CMOS Combinational Digital Gates.
CO.3. Designing of Industry Standard TG based Sequential Digital Gates.
CO.4. Learning High Level Synthesis in EDA flow.
CO.5. Learning Logic Synthesis in EDA flow and Verilog RTL.
CO.6. Learning Physical Place and Route in EDA flow.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question