DIGITAL LOGIC
(ECEN 2104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The 2's complement representation of $(-19)_{10}$ is
(a) 101100 (b) 101110 (c) 101101 (d) none of these.

(ii) An example of reflected code is
(a) BCD (b) GRAY (c) ASCII (d) Hamming code.

(iii) The equivalent binary number for the gray number 1011010 is
(a) 1111111 (b) 1000000 (c) 1101100 (d) 1011101.

(iv) The equivalent octal number for the hexadecimal number $(2A.B2)_H$ is
(a) $(52.544)_8$ (b) $(62.775)_8$ (c) $(53.670)_8$ (d) $(32.436)_8$.

(v) Simplified form of Boolean expression $(A + \bar{B} + \bar{A}B)C$ is
(a) 1 (b) 0 (c) C (d) $\bar{C}$.

(vi) The disabling logic for OR gate is
(a) 0 (b) 1 (c) all of the above (d) none of the above.

(vii) A XNOR gate can be made to act as NOT gate by
(a) by setting one of the Inputs at 0 (b) by setting one of the Inputs at 1
(c) by shorting the Inputs and the Output (d) all of the above.

(viii) In JK flip flop with NAND gates only, for CLK = 1, J = 1, K = 0, the output is
(a) No change in state (b) Reset State
(c) Toggle State (d) Set State.

(ix) Which logic family has minimum power dissipation ?
(a) RTL (b) CMOS (c) DTL (d) TTL.

(x) If an asynchronous counter have 3 identical flip-flops with t_{pd} = 50 ns, then what is the total propagation delay and the maximum frequency?
(a) 150 ns & 6.67 MHz (b) 160 ns & 5.67 MHz
(c) 140 ns & 2.23 MHz (d) None of these.

Group - B

2. (a) (i) Represent $(5489)_{10}$ in Gray code.
(ii) Represent $(572.61)_8$ in common binary code
(iii) Realize $Y = \overline{AB} + A + \overline{(B + C)}$ using NAND gates only.
[(CO1)(Evaluate/HOCQ)]

(b) Simplify the following Boolean function using K-map:
$f(A, B, C, D) = \sum m(0,1,4,5,9,11,14,15) + \sum d(10,13)$. [(CO1)(Evaluate/HOCQ)]

(3 + 3 + 3) + 3 = 12

3. (a) Perform the following conversions
(i) $(1011.1010)_2$ to Decimal
(ii) $(77.625)_{10}$ to Octal
(iii) $(2A.F6)_H$ to Octal
(iv) $(23.46)_8$ to Hexadecimal. [(CO1)(Understand/LOCQ)]

(b) State the following :- (i) DeMorgan's Theorem (ii) Distributive Law.
[(CO1)(Remember/LOCQ)]

(c) Derive the logic expression for the function:
Y = F(A, B, C, D) = $\pi_M(0, 3, 6, 9, 12, 15)$ by Tabular Method and draw the corresponding logic circuit. [(CO1)(Apply/IOCQ)]

4 + 2 + 6 = 12

Group - C

4. (a) Realize a full subtractor circuit using half subtractor module and necessary logic gates. [(CO1)(Remember/IOCQ)]

(b) Realize a full adder circuit using 4:1 multiplexer. [(CO1)(Evaluate/HOCQ)]

6 + 6 = 12

5. (a) Design a 1-bit Comparator circuit. [(CO1)(Apply/IOCQ)]

(b) Draw the logic circuit of 3-bit Odd-cum-Even Parity Generator and Checker circuit.
[(CO1)(Apply/IOCQ)]

(c) Implement 8:1 Multiplexer by 4:1 Multiplexer. [(CO1)(Analyze/IOCQ)]

3 + 4 + 5 = 12

Group - D

6. (a) Design a synchronous mod-5 counter using J-K flip-flop. [(CO2)(Create/HOCQ)]

(b) Among synchronous counter and asynchronous counter which one is faster and why? [(CO2)(Remember/LOCQ)]

(c) Realize a 3 bit ring counter and explain its operation with proper timing diagram.
[(CO2)(Analyse/IOCQ)]

6 + 2 + 4 = 12

7. (a) Convert SR flip flop to :- (i) D flip flop (ii) JK flip flop. [(CO2)(Apply/IOCQ)]

(b) What is Race Around condition? How is it eliminated? [(CO2)(Understand/LOCQ)]

(c) State the differences between combinational logic circuit and sequential logic circuit. [(CO2)(Remember/LOCQ)]

6 + 4 + 2 = 12

Group - E

8. (a) Design a basic 2 input TTL NAND gate and explain. [(CO5)(Remember/IOCQ)]
   (b) Implement the function $Y = \overline{(A + B)}$ using CMOS logic circuit. [(CO4)(Apply/IOCQ)]

6 + 6 = 12

9. Write short notes (any 2):
   (i) Master-Slave Flip flop
   (ii) 4-bit BCD adder
   (iii) 4-bit even parity generator and checker. [(CO1)(Remember/LOCQ)]

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	27.08	47.92	25

Course Outcome (CO):

After the completion of the course students will be able to
1. Learn Binary Number system and logic design using combinational gates.
2. Design applications of Sequential Circuits.
3. Design Finite State Machines.
4. Learn Memory classifications.
5. Learn basics of CMOS logic.
6. Learn various digital component design as used in VLSI applications.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question