(vi) Propagation delay of a logic gate can be measured by
(a) crystal oscillator (b) ring counter
(c) ring oscillator (d) none of the above.

(vii) A classification of ICs with complexities of 100 to 1000 equivalent gates on a chip is known as
(a) SSI (b) MSI (c) LSI (d) VLSI.

(viii) How many flip-flops are required to make a MOD-30 binary counter?
(a) 15 (b) 6 (c) 5 (d) 30.

(ix) The terminal count of a typical modulus-15 binary counter is _____
(a) 1000_2 (b) 1110_2 (c) 1011_2 (d) 1101_2.

(x) A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is
(a) constantly low (b) constantly high
(c) a 20 kHz square wave (d) a 10 kHz square wave.

Group - B

2. (a) Realize (i) a buffer and an inverter by using XOR gate.
(ii) an OR gate by using only NAND gate.

(b) Convert (324.576)8 = (? ?)16

(c) What is the difference between combinational and sequential circuit?

(d) Design a 4-bit full adder-subtractor circuit.

2 + 2 + 2 + 6 = 12

3. (a) Realize an 8:1 multiplexer by using 2:1 multiplexer.

(b) Implement the logic function Y(A,B,C,D) = ∑m(1,4,5,7,9,12,13) by using 4:1 multiplexer.

4 + 8 = 12

Group - C

4. (a) Minimize the logic function Y(A,B,C,D,E) = ∑m(0,2,3,5,7,8,10,11,14,1516,18,24,26,27,29,30,31) by using Karnaugh map.

(b) Design an S-R flip flop with truth table by using only NAND gates.

8 + 4 = 12

5. (a) Design a frequency divider where output frequency, f_0 is divided by 16 of clock frequency.

(b) Design a MODULO-8 synchronous counter and explain with output waveforms.

6 + 6 = 12

Group – D

6. (a) Design a ripple counter to start the count at zero and stop the count at 5 and start the count again from zero.

(b) Write short note on Ring counter.

7 + 5 = 12

7. (a) Write short note on Johnson counter.

(b) Implement the given functions using programmable logic array (PLA)
W(a,b,c)= $\sum m(0,2)$, X(a,b,c)= $\sum m(0,3,4)$, Y(a,b,c)= $\sum m(3,4,5,7)$.

4 + 8 = 12

Group - E

8. (a) Compare between logic Families: TTL, ECL, and CMOS

(b) Write short notes on Successive-approximation type ADC and Binary weighted DAC.

6 + 6 = 12

9. (a) Implement the following logic functions by using PROM.
X= $\sum m(0,1,3,7,9)$, Y= $\sum m(2,4,6,7,12)$

(b) Design A NAND gate using CMOS logic.

7 + 5 = 12

B.TECH/AEIE/4TH SEM /AEIE 2201/2016
2016

DIGITAL ELECTRONIC CIRCUITS
(AEIE 2201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following: **10 × 1 = 10**

(i) Which of the following statements does not describe an advantage of digital technology?
(a) The values may vary over a continuous range
(b) The circuits are less affected by noise
(c) The operation can be programmed
(d) Information storage is easy.

(ii) A full subtractor circuit requires _____.
(a) two inputs and two outputs
(b) two inputs and three outputs
(c) three inputs and one output
(d) three inputs and two outputs.

(iii) (r-1)'s complement of a number 'N' having 'n' digit is
(a) (r^n-1)-N (b) $(r-1)^n$-N
(c) $(r+1)^n$-N (d) None of the above.

(iv) A flip-flop has _____.
(a) one stable state (b) no stable states
(c) two stable states (d) none of the above.

(v) Decimal equivalent of the fractional binary number 0000.1010 is
(a) 0.625 (b) 0.50 (c) 0.55 (d) 0.10.