M.TECH/VLSI/2ND SEM/VLSI 5202/2022

VLSI DESIGN, TESTING AND VERIFICATION
(VLSI 5202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The output of physical design is
(a) Layout (b) Veriog (c) RTL (d) Circuit.

(ii) In Die Variation (IDV) means variation
(a) Lot to Lot (b) Inside die (c) Within Wafer (d) Wafer to Wafer.

(iii) Data refresh operation is needed in
(a) DRAM (b) EROM (c) EEPROM (d) SRAM.

(iv) Which among the following has the highest gate integration capacity?
(a) FPGA (b) CPLD (c) PLD (d) ASIC.

(v) VHDL is a
(a) Multi-threaded program (b) C like programming language
(c) Single user program (d) Sequential program.

(vi) Scan Design is needed to test
(a) Sequential Circuit (b) Combinational Circuit
(c) Stuck at Faults (d) None of above.

(vii) Smallest size Memory cell is
(a) DRAM (b) SRAM
(c) Register File (d) Flip-Flop.

(viii) Logic Synthesis translates descriptions from
(a) Physical to Behavioural (b) Structural to Physical
(c) Behavioural to Structural (d) Structural to Behavioural.

(ix) With Technology advancement, via contact resistance
(a) Increases (b) Decreases
(c) Remains same (d) Hard to say.

(x) The critical path for a design refers to
(a) The path having maximum delay (b) The path with minimum delay
(c) The path with optimum delay (d) The path with no delay.

Group- B

2. (a) Explain briefly under what PVT condition, NMOS Transistor behaves fastest and why. [(CO5)(Analyze/IOCQ)]
(b) Explain how H-Tree Clock Network helps to reduce clock skew. [(CO5)(Analyze/IOCQ)]
6 + 6 = 12

3. (a) Explain write '1' followed by read '1' operation in 1-Transistor DRAM Circuit using circuit diagram and timing waveforms. [(CO1)(Analyze/IOCQ)]
(b) Explain sizing criteria of 6 Transistor SRAM cell. [(CO1)(Analyze/IOCQ)]
6 + 6 = 12

Group - C

4. (a) Briefly explain components of interconnect capacitance. [(CO2)(Understand/LOCQ)]
(b) Why driver side of a wire needs to be low resistance and receiver side of the wire needs to be low capacitance, explain using Elmore Delay model. [(CO2)(Analyze/IOCQ)]
6 + 6 = 12

5. (a) Explain Static Timing Analysis. [(CO3)(Understand/LOCQ)]
(b) Explain PVT corner and worst case design criteria. [(CO3)(Analyze/IOCQ)]
6 + 6 = 12

Group – D

6. (a) For a flip flop based sequential circuit, Cycle Time = 200ps, Setup Time = 25ps, Clock-Skew = 20ps, Combinational Delay = 70ps, Clock to Out Delay of Flop = 40ps. Hold Time = 50ps. What is setup margin and hold margin for the Circuit? [(CO4)(Evaluate/HOCQ)]
(b) Define clock skew and what are sources of Clock Skew? [(CO5)(Remember/LOCQ)]
6 + 6 = 12

7. (a) What is best circuit scheme to create 8 to 256 bit decoder, explain with diagram. [(CO1)(Evaluate/HOCQ)]
(b) For a memory block of 256 Kb memory bits and 32 data bits, explain how many row address bits and how many column address bits are needed. [(CO1)(Evaluate/HOCQ)]
6 + 6 = 12

Group – E

8. (a) What is input test pattern to detect Stuck-at-1 fault at the output of a 2 input NAND gate ? [(CO6)(Evaluate/HOCQ)]
   (b) Explain D-Algorithm using an example. [(CO6)(Analyze/IOCQ)]

6 + 6 = 12

9. (a) Explain how Level Sensitive Scan Design Flip Flop (LSSD-SFF) works using circuit diagram. [(CO6)(Analyze/IOCQ)]
   (b) Generate primary input test patterns (i) for S-a-0 fault at output of 3 input NOR Gate and (ii) for S-a-1 fault at output of 3 input NAND Gate. [(CO6)(Evaluate/HOCQ)]

6 + (3 + 3) = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	18.75	50.00	31.25

Course Outcome (CO):

After the completion of the course students will be able to
1. Students will learn embedded Memory Design in VLSI Chip
2. Students will learn VLSI Interconnect Design
3. Students will learn Industry Standard STA (Static Timing Analysis) Method
4. Students will learn Set-up and hold Checks for Timing Verification
5. Students will learn process variation and Clock skew concepts
6. Students will learn Si Testing/Debug Methods

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question