M.TECH/VLSI/2ND SEM/VLSI 5232/2022

LOW POWER VLSI DESIGN
(VLSI 5232)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Maximum leakage power contribution comes from
(a) channel leakage (b) gate leakage of ON transistor
(c) junction leakage (d) gate leakage of OFF transistor.

(ii) Low power VLSI circuit design is necessary due to
(a) increase in transistor count (b) high speed of operation
(c) increase in leakage current (d) all of the above.

(iii) Dynamic power dissipation includes
(a) switching power dissipation
(b) diode leakage current
(c) glitching power, switching power and short circuit power
(d) subthreshold leakage.

(iv) The power dissipation of a circuit that takes place when it is not active is called the
(a) dynamic power dissipation (b) static power dissipation
(c) in active power dissipation (d) none of the above.

(v) In a generic CMOS circuit, when the load capacitance charges, power is dissipated through the
(a) pull up network only (b) pull down network only
(c) pull up and pull down networks (d) itself.

(vi) If threshold voltage of transistor is increased 2x, dynamic power of digital gate
(a) decreases 2x (b) increases 2x
(c) remains Same (d) increases 4x.

(vii) The most important parameter to reduce the short circuit power dissipation is
(a) V_{dd} (b) frequency, f
(c) rise time, τ (d) gate length.

(viii) If rise time of input of an inverter is increased, then short circuit current
(a) increases linearly (b) decreases linearly
(c) remains same (d) decreases exponentially.

(ix) Glitch power can be reduced by implementing
(a) cascaded form (b) balanced form
(c) inserting buffers (d) both (b)and (c).

(x) Both power and delay reduction for a digital gate is possible if
(a) CL decreases (b) V_{DD} decreases
(c) activity factor decreases (d) never possible.

Group- B

2. (a) What is short circuit power dissipation in CMOS circuits? [(CO4)(Remember/LOCQ)]
(b) Outline the cause of origin of short circuit power dissipation in the CMOS circuits. [(CO2)(Understand/LOCQ)]
(c) Develop an expression for the short circuit power and analyze the possible means of reducing it. [(CO1)(Analyze/IOCQ)]
1 + 1 + 10 = 12

3. (a) What do you understand by switching activity? [(CO2)(Understand/LOCQ)]
(b) Obtain the expression for the switching activity of a gate with equiprobable inputs. [(CO3)(Create/HOCQ)]
(c) Hence show the dependence of switching power dissipation on the fan-in of a gate. [(CO4)(Analyze/IOCQ)]
2 + 8 + 2 = 12

Group - C

4. (a) What is subthreshold leakage current? [(CO4)(Understand/LOCQ)]
(b) Briefly explain three mechanisms that affect subthreshold leakage current. [(CO2)(Understand/LOCQ)]
(c) Name the two possible pn-junction leakage mechanisms that lead to standby power dissipation in a CMOS circuit. [(CO1)(Understand/LOCQ)]
2 + 9 + 1 = 12

5. (a) Show how VTCMOS circuits help to reduce the subthreshold leakage current. [(CO2)(Analyze/IOCQ)]
(b) Identify the disadvantage of using VTCMOS circuits. [(CO3)(Apply/IOCQ)]
10 + 2 = 12

Group - D

6. (a) Distinguish between standby leakage power and runtime leakage power dissipation. [(CO4)(Understand/LOCQ)]

(b) Explain how MTCMOS techniques may be used for leakage power reduction. [(CO2)(Apply/IOCQ)]

(c) Mention the factors that affect the speed performance of MTCMOS circuits. [(CO1)(Remember/IOCQ)]

2 + 8 + 2 = 12

7. (a) What are the various components of Load Capacitance (CL) in digital circuits? [(CO4)(Remember/LOCQ)]

(b) Illustrate with a suitable example the occurrence of glitch power. [(CO3)(Understand/LOCQ)]

(c) How can it be minimized? [(CO1)(Apply/IOCQ)]

6 + 5 + 1 = 12

Group - E

8. (a) Distinguish between constant-field and constant-voltage feature size scaling. [(CO4)(Remember/LOCQ)]

(b) Compare their advantages and disadvantages. [(CO3)(Understand/LOCQ)]

(c) Compare the constant-field and constant-voltage scaling approaches in terms of the area, delay and power density parameters. [(CO4)(Analyse/IOCQ)]

2 + 4 + 6 = 12

9. (a) What is parallel processing? [(CO4)(Remember/LOCQ)]

(b) What are the advantages of using a parallel architecture in VLSI design? [(CO3)(Understand/IOCQ)]

(c) Show how parallelism can be used to achieve low power instead of high performance in realizing a 16 bit adder circuit. [(CO4)(Apply/IOCQ)]

1 + 1 + 10 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	37.5	54.17	8.33

Course Outcome (CO):

After the completion of the course students will be able to

1. Students will learn source of CMOS Dynamic Power Dissipation
2. Students will learn CMOS Dynamic Power Reduction Techniques
3. Students will learn source of CMOS Standby (leakage) Power Dissipation & Reduction Techniques
4. Students will learn Short Circuit Power Reduction Techniques
5. Students will learn Embedded Memory Power Reduction Techniques
6. Students will learn System and Architecture level Power Reduction Techniques