M.TECH/VLSI/2ND SEM/VLSI 5201/2022

ANALOG VLSI IC DESIGN
(VLSI 5201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) In a sample-and-hold circuit, the minimum sample and hold time is
(a) $T_{sample} = t_{settling} + t_{acquisition}$ (b) $T_{sample} = t_{settling}$
(c) $T_{sample} = t_{acquisition}$ (d) $T_{sample} = t_{settling} + t_{acquisition} + T_{clock}$.

(ii) For a MOS diode
(a) channel transconductance becomes channel conductance if $(W/L)_p=2(W/L)_N$
(b) channel transconductance becomes channel conductance if $V_{DS} \leq (V_{GS} - V_{th})$
(c) channel transconductance becomes channel conductance
(d) None of the above.

(iii) A good current mirror should have
(a) Non-identical drain-source voltages and high output resistance
(b) Identical drain-source voltages and high output resistance
(c) Non-identical drain-source voltages and low output resistance
(d) Identical drain-source voltages and low output resistance

(iv) The resistance between the drain and source terminal is proportional to
(a) λ (b) λ^2 (c) $(1/\lambda^2)$ (d) $(1/\lambda)$.

(v) The frequency of the signal applied to the switched-capacitor circuit should satisfy the criteria
(a) $f_{signal} << f_{clock}$ (b) $f_{signal} >> f_{clock}$ (c) $f_{signal} = 2f_{clock}$ (d) $f_{clock} = 2f_{signal}$.

(vi) The higher sampling speed is achieved by
(a) small aspect ratio of the MOSFET and small sampling capacitor
(b) large aspect ratio of the MOSFET and small sampling capacitor
(c) large aspect ratio of the MOSFET and large sampling capacitor
(d) small aspect ratio of the MOSFET and large sampling capacitor.

(vii) An *n*-MOSFET can operate as a diode when
(a) gate and source terminals are shorted
(b) gate and drain terminals are shorted
(c) substrate and source terminals are shorted
(d) source to substrate voltage is equal to V_{th}.

(viii) The dynamic impact of the op-amp on the *DAC* performance can come from the
(a) unity gain bandwidth (b) settling time
(c) slew rate (d) All of the above.

(ix) An ideal differential amplifier should have *CMRR*
(a) $0 < CMRR < 1$ (b) One
(c) Infinite (d) Zero.

(x) The *PSRR* of the op-amp is given by
(a) $PSRR = \frac{\Delta V_{DD}}{\Delta V_{out} A_v(S)}$ (b) $PSRR = \frac{A_v(S)\Delta V_{out}}{\Delta V_{DD}}$
(c) $PSRR = \frac{A_v(S)\Delta V_{DD}}{\Delta V_{out}}$ (d) None of the above.

Group- B

2. (a) Explain the input – output characteristics of a basic resistive load differential amplifier circuit. [(CO2)(Understand/LOCQ)]
(b) Deduce the *ICMR* of this type of circuit. [(CO2)(Analyse/IOCQ)]
(c) Consider the circuit in Fig.1 in which *M2* is twice as wide as *M1*. Calculate the small-signal gain if the bias values of V_{in_1} and V_{in_2} are equal. [(CO2)(Evaluate/HOCQ)]

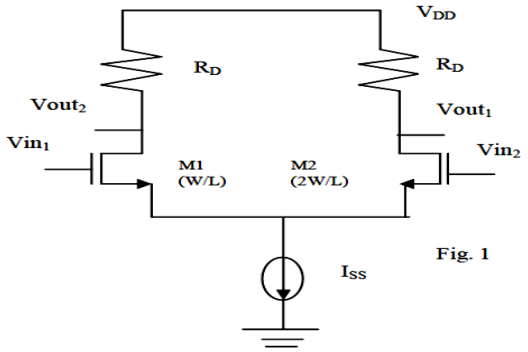

Fig. 1

4 + 5 + 3 = 12

3. (a) Briefly explain the current-voltage characteristics of a current sink and source. [(CO1)(Understand/LOCQ)]
(b) Derive the small-signal voltage gain of a push-pull amplifier from its small-signal equivalent circuit. [(CO2)(Analyze/IOCQ)]
(c) Estimate the gain and high frequency response of an *NMOS* transistor fabricated in the *0.25μm CMOS* process with $L = 0.4\mu m$. Let the transistor be operated at $V_{ov} = 0.25V$. Find (W/L) that is required to obtain $I_D = 10\mu A, 100\mu A$ *and* $1mA$. At each value of I_D, determine g_m, r_0, A_0, C_{gs}, C_{gd}, and f_T. Also, for each value of I_D, evaluate the gain-bandwidth product (f_t) of a common-source amplifier loaded by a *1pF*,

capacitance, neglecting the internal capacitances of the transistor.

[(CO2)(Evaluate/HOCQ)]

4 + 5 + 3 = 12

Group – C

4. (a) Briefly discuss the effects of nonlinearity in RF circuits.

[(CO3)(Understand/LOCQ)]

(b) An analog multiplier mixes its two inputs $x_1(t)$ and $x_2(t)$, ideally producing output $y(t) = kx_1(t)x_2(t)$, where k is a constant. Assume, $x_1(t) = A_1Cos\omega_1 t$ and $x_2(t) = A_2Cos\omega_2 t$.

(i) If the mixer is ideal, determine the frequency components.

(ii) If the input port sensing $x_2(t)$ suffers from third-order nonlinearity, determine the output frequency components. [(CO3)(Apply/IOCQ)]

(c) In most circuits, one terminal of the inductor(s) is at *ac* ground. Which terminal of the structure should be grounded in this Fig.2. [(CO3)(Evaluate/HOCQ)]

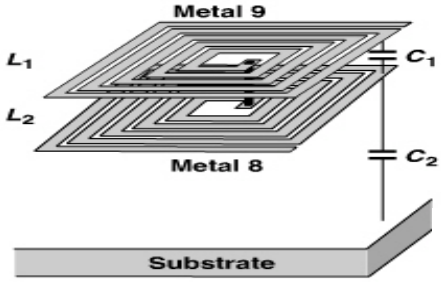

Fig.2

4 + 5 + 3 = 12

5. (a) Briefly discuss the critical attributes of varactors in oscillator design.

[(CO3)(Understand/LOCQ)]

(b) Analyze the variation of the Q of *MOS* varactors with capacitance and the effect of overlap capacitance on the varactor capacitance range.

[(CO3)(Analyze/IOCQ)]

(c) Prove that the Q of the circuit modelling inductor losses by both series and parallel resistors is given by $Q = \frac{L_1\omega R_P^{'}}{L_1^2\omega^2 + R_S^{'}(R_S^{'}+R_P^{'})}$ where the notations have their usual significance. [(CO3)(Evaluate/HOCQ)]

4 + 5 + 3 = 12

Group - D

6. (a) Briefly explain quantization error of *ADC*. [(CO4)(Understand/LOCQ)]

(b) Design a 3-bit flash *ADC* listing the values of the voltages at each resistor tap assuming $V_{REF} = 5V$. [(CO4)(Analyze/IOCQ)]

(c) Construct a table evaluating the values of the thermometer code and the output of the decoder for $V_{in} = 1.5\ V, 3.0\ V$ and $4.5V$. [(CO4)(Create/HOCQ)]

4 + 5 + 3 = 12

7. (a) Explain the principle of operation of serial charge redistribution *DAC*.

[(CO4)(Remember/LOCQ)]

(b) The digital word to be converted using this type of *DAC* is given as $b_0 = 1$, $b_1 = 1$, $b_2 = 0$, and $b_3 = 1$. Assume, $C_1 = C_2$ and determine the conversion of this digital input word. [(CO4)(Analyze/IOCQ)]

(c) Draw the waveform of voltages V_{C_1} and V_{C_2} evaluated with proper labelling. [(CO4)(Evaluate/HOCQ)]

4 + 5 + 3 = 12

Group – E

8. (a) Briefly explain the basic building blocks of the switched capacitor circuits. [(CO5)(Understand/LOCQ)]

(b) Derive the transfer function of parasitic sensitive integrator. [(CO5)(Analyse/IOCQ)]

(c) Evaluate the equivalent resistance of a *5pF* capacitance sampled at a clock frequency of 100KHz. [(CO5)(Evaluate/HOCQ)]

4 + 5 + 3 = 12

9. (a) Explain the Barkhausen criteria for oscillation. [(CO6)(Understand/LOCQ)]

(b) Analyze the stability of single-pole amplifier system with proper graphical illustration. Also, comment whether it can oscillate or not. [(CO6)(Analyze/IOCQ)]

(c) Evaluate the minimum required voltage gain per stage in four-stage ring oscillator. How many signal phases are provided by the circuit? [(CO6)(Evaluate/HOCQ)]

4 + 5 + 3 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	33.33	41.67	25

Course Outcome (CO):

After the completion of the course students will be able to

1. Understand and analyze MOS-based analog VLSI sub-circuits, relevant small-signal equivalent circuit models and design them *eg.* Current mirrors.
2. Design and analyze MOS circuits of practical importance *eg*. Common-source amplifiers and differential amplifiers.
3. Understand the basic concepts in RF design and the geometry, models of passive devices used in RFIC.
4. Understand the principle of operation, characterization of the data converter circuits and design them.
5. Understand and analyze different topologies of switched-capacitor circuits and apply the concept for the analysis of circuits of practical applications.
6. Understand the principle of operation of the oscillator circuit and apply the concept for the analysis of circuits of practical applications.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question