M.TECH/VLSI/2ND SEM/VLSI 5241/2022

ADVANCED VLSI PROCESSOR
(VLSI 5241)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Instruction ADD R1, [1000h] belong to which of the following architecture?
(a) L/S (b) R/M (c) R+M (d) L?M.

(ii) In which addressing mode the effective address of the operand is generated by adding a constant value to the contents of the register.
(a) Immediate (b) Direct
(c) Indexed (d) Indirect.

(iii) The _____ architecture is a computer architecture with separate storage and signal pathways for instructions and data. It contrasts with the _____ architecture, where program instructions and data share the same memory and pathways.
(a) Harvard, Von Neumann (b) RISC, CISC
(c) Von Neumann, Harvard (d) ARM, INTEL

(iv) The basic instruction cycle consists of the three stages in sequence
(a) Decode -> Fetch -> Execute (b) Fetch -> Decode -> Execute
(c) Execute -> Decode -> Fetch (d) Execute -> Fetch -> Decode.

(v) A control memory is used to store _____ micro instructions.
(a) hardwired (b) micro-coded
(c) stack oriented (d) move related

(vi) The Micro-instructions are stored in
(a) main memory (b) control memory
(c) flash memory (d) cache memory.

(vii) The CMAR (Control Memory Address Register) is used when the CU (Control Unit) design type is
(a) hard wired (b) firm wired
(c) micro-programmed (d) soft wired.

(viii) Thumb instruction set belongs to which architecture family?
(a) Intel Polaris (b) DSP chip TMS320C5X
(c) ARM (d) DSP5600X from MOTOROLA

(ix) In ARM architecture register R15 is used as
(a) link register (b) stack pointer
(c) program counter (d) status register.

(x) Status Registers ST0 and ST1 are of size
(a) 8 bits each (b) 16 bits each
(c) 8 bits and 16 bits (d) 16 bits and 8 bits.

Group - B

2. (a) Sketch the instruction format of a two address intruction that uses immediate, register direct and indexed addressing mode if size of the memory is 1 MB and size of instruction word is limited to 16 bits with 3 bit opcode field. [(CO1)(Analyze/LOCQ)]

(b) The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A two word call subroutine instruction is located in memory at address 1120 followed by the address field of 6720 at location 1121. What are the content of PC, SP, and the top of the stack?, A) Before the call instruction is fetched from memory?, B) After the call instruction is executed?, C) After the return from subroutine? [(CO1)(Analyze/HOCQ)]

6 + 6 = 12

3. (a) Explain the difference between RISC and CISC architecture with examples. [(CO2)(Remember/LOCQ)]

(b) Consider the following register transfer statements for two four bit registers R1 and R2

xT : R1 ← R1 + R2
x'T : R1 ← R1

Draw a hardware implementation of the two statements using two registers, a 4 bit adder, and a quadruple 2 to 1 line multiplexer. [(CO1)(Understand/HOCQ)]

6 + 6 = 12

Group - C

4. (a) Find the RAW, WAR and WAW, and potential control hazards in the following code

```
        LOAD R1 ← M[312]
        ADD R2 ←R2 + R1
        JC   LABEL1
        ADD R3 ←R3 + 1
        STORE R2 ← R1 + R3
LABEL1: STORE R1 ← R2+ R3.
```

[(CO3)(Analyze/IOCQ)]

(b) A non-pipeline takes 40ns to complete a task. The same task can be processed in 4 segment pipeline with a clock cycle of 4ns. Determine the speed up ratio of the pipe line for 50 tasks. What is the maximum speed up that can be achieved in this case? [(CO3)(Apply/IOCQ)]

6 + 6 = 12

5. (a) Explain how convolution is performed using a single MAC unit of TMS320C5x. [(CO3)(Understand/LOCQ)]

(b) Why use of DARAM helps with speedup? [(CO3)(Understand/LOCQ)]

(c) Initially let the content of data memory location 1500h be 678Ah, and content of register R0 be C234h. Describe the content of the register R0 and mem location 1500h after execution of instruction
(i) LMMR AR0, #1500
(ii) SMMR AR0, #1500. [(CO3)(Analyze/IOCQ)]

4 + 4 + 4 = 12

Group - D

6. (a) Describe with example what is a hardware accelerator? What is the difference between an accelerator and a coprocessor? [(CO4)(Remember/LOCQ)]

(b) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct, (b) immediate, (c) relative, (d) register indirect, (e) index with R1 as the index register. [(CO4)(Analyze/IOCQ)]

6 + 6 = 12

7. (a) Describe the ARM7 register structure and the processor modes. Mention the use of R13 - R15 and SPSR. [(CO4)(Remember/LOCQ)]

(b) What are four ARM cortex series processor? What are their applications? [(CO4)(Understand/LOCQ)]

(c) Given a 32X8 ROM with an enable input, show the external connections necessary to construct a 128 × 8 ROM with four chips and a decoder. [(CO4)(Analyze/IOCQ)]

4 + 4 + 4 = 12

Group - E

8. (a) What is fine and coarse grained granularity in terms of parallel programming and data usage? [(CO5)(Remember/LOCQ)]

(b) Describe the limitations of an uniprocessor, and discuss how CMPs are used to overcome them. [(CO5)(Understand/LOCQ)]

6 + 6 = 12

9. (a) Classify the uni and multi processors following Flynns Taxonomy. [(CO6)(Remember/LOCQ)]

(b) What is UMA and NUMA? What are their relative pros and cons?
[(CO6)(Understand/LOCQ)]

(c) Explain what is a multithreaded processor with its different types.
[(CO6)(Analyse/IOCQ)]

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	56.25	31.25	12.5

Course Outcome (CO):

After the completion of the course students will be able to
1. Students will learn basic structure of instruction set architecture (ISA)
2. Students will learn CISC and RISC Architecture
3. Students will learn sample DSP Processor Architecture
4. Students will learn Accelerator
5. Students will learn Multi-Threaded Processor
6. Students will learn use of Microprocessor cores in SOC Design

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question