M.TECH/VLSI/2ND SEM/VLSI 5242/2022

ADVANCED NANO DEVICES
(VLSI 5242)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Subthreshold swing of a MOSFET
(a) decreases with depletion capacitance and increases with oxide capacitance
(b) decreases with depletion capacitance and decreases with oxide capacitance
(c) increases with depletion capacitance and decreases with oxide capacitance
(d) increases with depletion capacitance and increases with oxide capacitance.

(ii) Hot electron effect causes
(a) Oxide wear out and breakdown (b) Change in threshold voltage
(c) Finite gate current (d) All of the above.

(iii) V_{dd} scaling
(a) makes the device slow.
(b) decreases the threshold voltage of the device.
(c) makes the device fast.
(d) increases the cut – off frequency of the device.

(iv) Velocity saturation causes the short channel device to saturate for _____ values of V_{DS}.
(a) larger (b) smaller (c) moderate (d) very large

(v) If fixed positive charges are present in the gate oxide of an n – channel enhancement type MOSFET, it will lead to
(a) A decrease in the threshold voltage
(b) Channel length modulation
(c) An increase in substrate leakage current
(d) An increase in accumulation capacitance.

(vi) High-power circuits generally use higher values of
(a) Gate to source current (b) Drain to source current
(c) Drain current (d) Gate to source voltage.

(vii) A long – channel NMOS transistor is biased in the liner region VDS = 50 mV and is used as a resistance. Which one of the following statements is NOT correct?
(a) If the device width W is increased, the resistance decrease
(b) If the threshold voltage is reduced, the resistance decreases
(c) If the device length L is increased, the resistance
(d) If VGS is increased, the resistance increases.

(viii) The conduction of current I_D depends on
(i) Gate to source voltage (ii) Drain to source voltage
(iii) Bulk to source voltage (iv) Threshold voltage
(v) Dimensions of MOSFET
(a) Only (i) (b) Only (i), (ii) and (iii) (c) Only (v) (d) All of the mentioned.

(ix) Source and drain in nMOS device are isolated by _____
(a) a single diode (b) two diodes
(c) three diodes (d) four diodes.

(x) 2DEG results in high mobility because
(a) there is negligible impurity scattering (b) there is no scattering
(c) electrons are in a quantum well (d) none of these.

Group – B

2. (a) Derive the relationship between threshold voltage and supply voltage. What do you mean by sub-threshold conduction? [CO1/Evaluate/HOCQ]
(b) What is subthreshold swing? What is the limit of subthreshold swing and why? How subthreshold swing can be improved? [CO1/Evaluate/HOCQ]
(4 + 2) + 6 = 12

3. (a) Draw the energy band diagram of a MOS system. [CO1/Remember/LOCQ]
(b) Explain the band diagram for a MOSFET for different gate voltages. [CO1/Analyse/IOCQ]
(c) To design the width of a MOSFET such that a specified current is induced for a given applied bias, consider an ideal n-channel MOSFET with parameters L=1.25μm, μn=650cm2/V-S, Cox =6.9X10-8 F/cm2 and VT=0.65V. Design the channel width W such that ID (sat) =4mA for VGS=5V. [CO1/Evaluate/HOCQ]
3 + 4 + 5 = 12

Group – C

4. (a) Explain with the energy band diagram, the effect of metal work function engineering on the MOS systems. [CO1/Analyse/IOCQ]
(b) Explain how the step function in channel potential is beneficial for asymmetric MOS structure. [CO2/Create/HOCQ].
8 + 4 = 12

5. (a) Explain with suitable expression, how the Effective Oxide Thickness (EOT) improves the gate leakage currents. [CO2/Analyse/IOCQ]
   (b) What are the limitations of Effective Oxide Thickness and how it can be improved? [CO2/Understand/LOCQ]

6 + 6 = 12

Group – D

6. (a) Draw and explain MOSFET high frequency model. [CO1/Remember/LOCQ]
   (b) Derive the relationship between cut-off frequency and parasitic capacitor. [CO1/Evaluate/HOCQ]

6 + 6 = 12

7. (a) Explain non uniform dopant distribution. Why Double Gate (DG) can improve ON current as well as mitigate OFF current. [CO4/Understand/LOCQ]
   (b) Why undoped substrate is chosen for scaled DG MOSFETs? [CO4/Analyse/IOCQ]

(2 + 6) + 4 = 12

Group - E

8. (a) How SCE can be minimized by Underlap Source Drain MOS structure? [CO3/Analyse/IOCQ]
   (b) List the advantages offered by an SOI MOSFET over the bulk MOSFET. [CO3/Analyse/IOCQ]
   (c) Differentiate between Partially-depleted (PD) and Fully-depleted (FD) Silicon-on-insulator (SOI) MOSFETs. [CO3/Analyse/IOCQ]

3 + 3 + 6 = 12

9. (a) Explain with suitable band diagrams the different possible structures when a narrow band gap and a wide band gap material form a heterojunction. [CO5/Evaluate/HOCQ]
   (b) Compare between the 2DEG formed in a MOSFET and in a high electron mobility transistor (HEMT). [CO5/ Evaluate/HOCQ]
   (c) Explain the operation of a HEMT with the help of necessary diagram. [CO5/ Evaluate/HOCQ]

5 + 2 + 5 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	17.71	41.67	40.63

Course Outcome (CO):

1. Students will learn various leakage phenomena in advanced MOS
2. Students will learn High K Plus Metal Gate Technology for advanced Process Nodes

3. Students will learn SOI MOS device
4. Students will learn FinFET Devices like DGMOS, Tri-gate
5. Students will learn Hetero-Structures
6. Students will learn CNT, Graphene Device

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question