



# HERITAGE INSTITUTE OF TECHNOLOGY

M.Tech 1<sup>st</sup> Semester Examination. 2014 Session : 2014-15

Discipline : AEIE

Paper Code : AEIE5101 Paper Name : MICRO-ELECTRONIC DEVICES AND CIRCUITS

Time Allotted : 3 hrs

Full Marks : 70

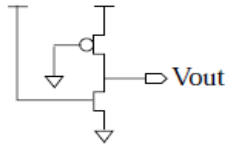
*Figures out of the right margin indicate full marks.*

*Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.*

*Candidates are required to give answer in their own words as far as practicable.*

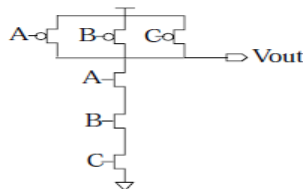
### Group – A (Multiple Choice Type Questions)

1. Choose the correct alternative for the following: 10 x 1=10
- (i) The threshold voltage of an n-channel MOSFET can be increased by:
- (a) Increasing the channel dopant concentration
  - (b) Reducing the channel dopant concentration
  - (c) Reducing gate oxide thickness
  - (d) Reducing the channel length
- (ii) In the circuit below, what is  $V_{out}$  equal to?



- (a)  $V_{DD}$
- (b) 0V
- (c)  $V_{DD}-V_t$
- (d) Not enough information

- (iii) The circuit given below



- computes what function of A, B, and C?
- (a) NAND
  - (b) NOR
  - (c) AND
  - (d) OR



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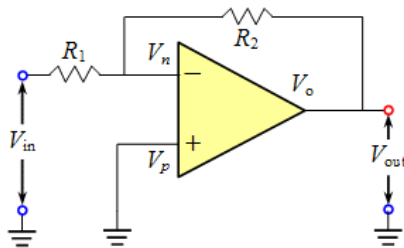
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- (iv) The extremely high input impedance of a MOSFET is primarily due to the
  - (a) absence of its channel
  - (b) negative gate-source voltage
  - (c) depletion of current carriers
  - (d) extremely small leakage current of its gate capacitor
  
- (v) What is the difference voltage output from an OpAmp if the inputs are an ideal in phase signal?
  - (a) the differential gain times twice the input signal
  - (b) the differential gain times the input signal
  - (c) the common-mode gain times twice the input signal
  - (d) the common-mode gain times the input signal
  
- (vi) An N-channel depletion mode MOSFET can be turned off by making VGS
  - (a) positive
  - (b) zero
  - (c) negative
  - (d) none of the above
  
- (vii) MOSFET input resistance is typically of the order
  - (a)  $10^{10}$ - $10^{15}\Omega$
  - (b)  $10^{10}$ - $10^{12}\Omega$
  - (c)  $10^{10}$ - $10^{21}\Omega$
  - (d) none

(viii)



If  $R_1 = 10\text{ k}\Omega$ , and  $R_2 = 30\text{ k}\Omega$ , the input impedance of the circuit is

- (a)  $10\text{ k}\Omega$
  - (b)  $40\text{ k}\Omega$
  - (c) infinity
  - (d) none of the above
- 
- (ix) Voltage follower is a special case of \_\_\_\_\_.
    - a) inverting configuration
    - b) non-inverting configuration
    - c) difference configuration
    - d) integrator configuration



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- (x) How does the average velocity of charge carriers vary with position along the channel of a modern MOSFET under large drain to source voltage?
  - a) The average velocity is constant from the source to the drain.
  - b) The average velocity increases from the source to the drain.
  - c) The average velocity decreases from the source to the drain.
  - d) The average velocity reaches a maximum between the source and the drain.

### Group - B

- 2.(a) Explain with diagram the CMOS implementation of a clocked SR flip-flop using pass-transistor and compare it with a standard CMOS flip-flop realization.
- (b) Describe the operation of a master-slave D flip-flop with the help of its circuit diagrams and two-phase non-overlapping clock wave forms. 5 + 7= 12
- 3.(a) Perform small signal analysis on a MOS cascade amplifier without the load circuit and derive an expression for voltage gain and output resistance.
- (b) Design a MOS cascade amplifier current source to provide a current of 100μA and an output resistance of 500kΩ. Assume the availability of a 0.18μm CMOS technology for which  $V_{DD}= 1.8V$ ,  $V_{tp}= -0.5V$ ,  $\mu_p C_{ox}= 90\mu A/V^2$  and  $V_A' = -5V/\mu m$ . Use  $|V_{ov}| = 0.3V$  and determine L and W/L for each transistor. 8 + 4= 12

### Group - C

- 4 (a) Describe how to convert a monostable multivibrator to an astable multivibrator using suitable circuit diagram?
- (b) For the circuit shown in Fig.1, let the op-amp saturation voltages be  $\pm 10V$ ,  $R_1=100k\Omega$ ,  $R_2=R=1M\Omega$  and  $C=0.01\mu F$ . Find the frequency of oscillation.

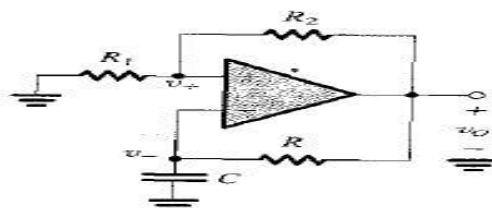


Fig.1

7 + 5= 12



# HERITAGE INSTITUTE OF TECHNOLOGY

M.Tech 1<sup>st</sup> Semester Examination. 2014 Session : 2014-15

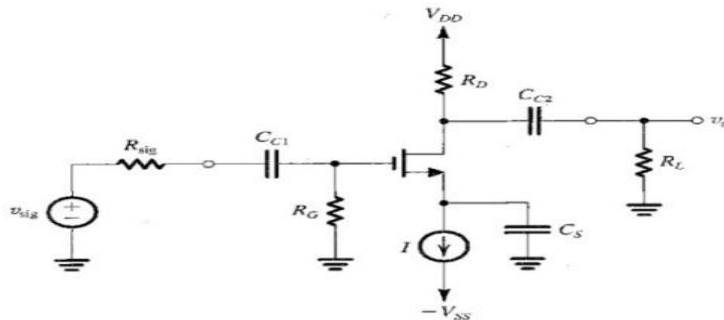
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- 5.(a) Perform analysis on a single OpAmp difference amplifier and derive an expression for its common and differential mode gains. Also comment on its differential input resistance.
- (b) It is required to connect a transducer having an open-circuit voltage of 1V and source resistance of 1MΩ to a load of 1kΩ resistance. Find the load voltage if the connection is done a) directly and b) through a unity gain voltage follower. 8 + 4= 12

### Group - D

- 6.(a) Perform small signal analysis on the given NMOS amplifier circuit, shown in following figure. Find an expression for output impedance and voltage gain.



- (b) Implement a switched capacitor filter circuit using OpAmp and derive an expression for its output resistance. 5 + 7= 12
- 7.(a) Explain the implementation of a monostable multivibrator using OpAmp and also derive an expression for time period of oscillation.
- (b) Compare a bipolar current mirror with MOS mirror. What is bias compensation in a bipolar mirror and how does it improve current transfer ratio. 7 + 3+2= 12



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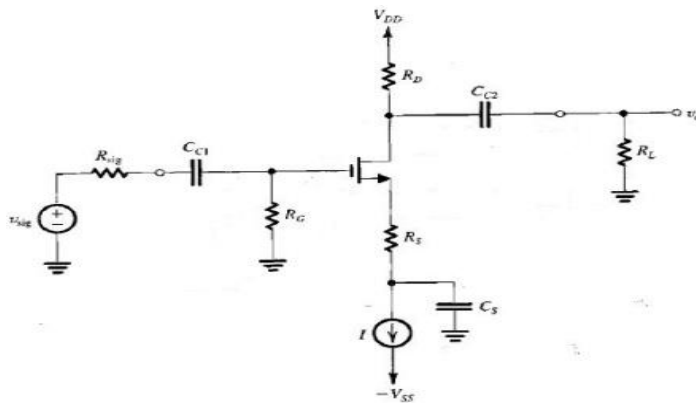
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### Group - E

8 (a) Perform small signal analysis on the common source amplifier, also find draw the equivalent circuit and deduce expressions for voltage gain, input and output impedances.



(b) Consider a CMOS inverter fabricated in a 0.18μm process for which V<sub>DD</sub>=1.8V, V<sub>tn</sub>=|V<sub>tp</sub>| = 0.5V, μ<sub>n</sub>=4μ<sub>p</sub>, and μ<sub>n</sub>C<sub>ox</sub>=300μA/V<sup>2</sup>. In addition, Q<sub>N</sub> and Q<sub>p</sub> have L=0.18μm and (W/L)<sub>n</sub>=1.5.

- i) Find W<sub>p</sub> that results in V<sub>M</sub>=V<sub>DD</sub>/2=0.9V. What is the silicon area utilized by the inverter in this case.
- ii) For the matched case above, find the values of V<sub>OH</sub>, V<sub>OL</sub>, V<sub>IH</sub>, V<sub>IL</sub> and noise margins NM<sub>L</sub> and NM<sub>H</sub>. For V<sub>i</sub>= V<sub>IL</sub>, find out the V<sub>o</sub>.
- iii) For the matched case above, find the values of output resistance for two inverter output states.

6 + 6= 12

9.(a) Implement the function  $Y = AB + \overline{A} \overline{B}$  using CMOS realization for OAI gates.

(b) Write short notes on any two of the following:

- a) Widlar current source
- b) Delay-Power product
- c) Input bias and offset currents in an OpAmp
- d) CMOS inverter circuit.

6 + (2x3) = 12