B.TECH/IT/4TH SEM/INFO 2203/2022

COMPUTER ORGANIZATION AND ARCHITECTURE
(INFO 2203)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Processor without structural hazard is
(a) faster (b) slower
(c) have longer clock cycle (d) have larger clock rate.

(ii) In devices, controller is used for _____
(a) buffering the data (b) manipulate the data
(c) calculate the data (d) input the data.

(iii) In case of, Zero-address instruction method the operands are stored in _____.
(a) Registers (b) Accumulators
(c) Push down stack (d) Cache

(iv) The addressing mode/s, which uses the PC instead of a general purpose register is____.
(a) indexed with offset (b) relative
(c) direct (d) both indexed with offset and direct

(v) The BOOT sector files of the system are stored in _____
(a) Harddisk (b) ROM
(c) RAM (d) Motherboard.

(vi) The pipelining process is also called as _____.
(a) Superscalar operation (b) Assembly line operation
(c) Von Neumann cycle (d) none of the mentioned

(vii) Prefetching is a solution for_____.
(a) data hazard (b) structural hazard
(c) control hazard (d) none of these

(viii) The situation wherein the data of operands are not available is called _____.
(a) Data hazard (b) Stock
(c) Deadlock (d) Structural hazard

(ix) Systolic array is an example of _____ architecture.
(a) MIMD (b) MISD (c) SIMD (d) SISD.

(x) The periods of time when the unit is idle is called as _____
(a) Stalls (b) Bubbles
(c) Hazards (d) Both Stalls and Bubbles.

Group- B

2. (a) Evaluate (-13) and (7) with the help of Booth Multiplication algorithm. [(CO3)(Evaluate/HOCQ)]

(b) X = (A*B)X(C/D)/E
Evaluate the above expression with the help of one address, two address and three address instructions. [(CO3)(Evaluate/HOCQ)]

6 + 6 = 12

3. (a) Draw and explain Von-Neumann architecture. (Explain each component). [(CO1)(Understand/LOCQ)]

(b) Justify that final carry in carry look ahead adder is only dependent on the carry generated in first adder. [(CO2)(Evaluate/HOCQ)]

8 + 4 = 12

Group - C

4. (a) Implement the bus connection with a CPU to connect four RAM chips of size 256 × 8 bits each and a ROM chip of size 256 × 8 bits. Assume the CPU has 8 bit data bus and 16 bit address bus. [(CO4)(Apply/IOCQ)]

(b) Define write back and write through policies in cache memory? [(CO4)(Remember/LOCQ)]

(c) Explain different types of locality of references in memory system. [(CO4)(Remember/LOCQ)]

5 + 2 + 5 = 12

5. (a) Discuss the limitation of direct mapped cache? [(CO4)(Understand/LOCQ)]

(b) Explain with an example how above mentioned limitation(s) can be improved in set-associative cache. [(CO4)(Explain/LOCQ)]

(c) A three level memory system having cache access time of 15 ns and disk access time of 80 ns has a cache hit ratio of 0.96 and main memory hit ratio of 0.9. Investigate what should be the main memory access time to achieve effective access time of 25 ns? [(CO4)(Create/HOCQ)]

3 + 4 + 5 = 12

Group - D

6. Consider the five- stage pipelined processor specified by the following reservation table.

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

(i) List the set of forbidden latencies and the collision vector.
(ii) Draw a state transition diagram showing all possible initial sequences (cycles) without causing a collision in the pipeline.
(iii) List all the simple cycles from the state diagram.
(iv) Identify the greedy cycles among the simple cycles.
(v) What is the minimum average latency (MAL) of this pipeline?

[(CO5)(Create/HOCQ)]
(2 + 4 + 2 + 2 + 2) = 12

7. (a) Discuss the working of VLIW processor in detail with suitable diagram. State the advantages and disadvantages of VLIW processor. [(CO5)(Remember/LOCQ)]
(b) What is instruction level parallelism (ILP)? Explain any two techniques that can be used for improving ILP with suitable examples as necessary.

[(CO5)(Understand/LOCQ)]
(4 + 4) + (1 + 3) = 12

Group - E

8. (a) Describe a superscalar RISC processor architecture consisting of an integer unit and a floating-point unit with diagram. [(CO6)(Remember/LOCQ)]
(b) Write down the advantages and disadvantages of Centralized shared memory architecture and distributed shared-memory architecture.

[(CO6)(Understand/LOCQ)]
6 + (3 + 3) = 12

9. (a) Describe the Omega, Baseline and Crossbar interconnection network with diagram. [(CO6)(Understand/LOCQ)]
(b) State the factors which affect the performance of an interconnection network.

[(CO6)(Analyze/IOCQ)]
(3 + 3 + 3) + 3 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	50	8.33	41.67

Course Outcome (CO):

After the completion of the course students will be able to

1. Describe and explain the difference between computer organization and computer architecture.
2. Design the ALU for different arithmetical and logical problems and apply the knowledge of different multiplication and division algorithm.
3. Formulate design methodology for using various types of instructions.
4. Differentiate between different Memory hierarchy (Primary, Secondary, Cache). Able to solve different kind of numerical based on memory technologies and page replacement techniques.
5. Differentiate between types of pipeline, hazards and selecting remedial techniques to handle the hazards. Able to distinguish between parallel architectures. Compare performance parameters of pipelines and deduce derivations to demonstrate change in performance parameters when branching is introduced. Able to solve numericals based on pipeline concepts.
6. Comparing techniques of ILP, types of CU, types of shared memory architectures. Distinguish between different multiprocessor architectures, Data Flow architecture, RISC and CISC architecture.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question