LOW POWER HIGH PERFORMANCE DIGITAL VLSI CIRCUIT DESIGN
(ECEN 4221)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) With Technology advancement via contact resistance
(a) increases (b) decreases
(c) remains same (d) hard to say.

(ii) Average wide delay is changing with Technology advancement in following way
(a) increasing (b) decreasing
(c) remaining same (d) increasing and then decreasing.

(iii) In Die Variation (IDV) means variation
(a) lot to lot (b) inside die
(c) within wafer (d) wafer to wafer.

(iv) If channel length of driver transistor is increased 2x, delay of digital gate
(a) decreases 2x (b) increases 2x
(c) decreases 4x (d) remains same.

(v) If P_A is signal probability of a input of inverter, the signal probability of inverter output is
(a) P_A (b) 1- P_A (c) 1 (d) 0.5.

(vi) From 65 nm onwards below power is maximum in a chip
(a) dynamic (b) leakage
(c) short circuit (d) contention.

(vii) The critical path for a design refers to
(a) the path having maximum delay (b) the path with minimum delay
(c) the path with optimum delay (d) the path with no delay.

(viii) Activity Factor is maximum for below circuit output
(a) memory node (b) dynamic
(c) static (d) clock.

(ix) For a Rising Edge Triggered D-Flip-Flop, if setup time is 200 ps and hold time is 50 ps, then input data needs to be stable for timing window of
(a) 200 ps (b) 50 ps (c) 150 ps (d) 250 ps

(x) Parasitic Extraction is done on
(a) verilog RTL (b) circuit netlist
(c) physical layout (d) all of them.

Group - B

2. (a) If P_A and P_B are Signal Probability of A and B input of an NOR gate, calculate Transition Probability of output Y of NOR gate. [(CO5)(Evaluate/HOCQ)]
(b) What are various techniques of Activity Factor reductions in digital Gate? [(CO5)(Understand/LOCQ)]
6 + 6 = 12

3. (a) Under what input condition Channel Leakage Power through a 3 input NOR Gate is minimum and why ? [(CO6)(Evaluate/HOCQ)]
(b) Under what PVT Condition, NMOS Transistor behave fastest way. [(CO4)(Analyze/IOCQ)]
6 + 6 = 12

Group - C

4. (a) For a flip flop based sequential circuit, Cycle Time = 400 ps, Setup Time = 50 ps, Clock-Skew = 40 ps, Combinational Delay = 270 ps, Clock to Out Delay of Flop = 60 ps. Hold Time = 70 ps. What is setup margin and hold margin for the Circuit? [(CO2)(Evaluate/HOCQ)]
(b) Define clock skew and what are sources of Clock Skew? [(CO4)(Understand/LOCQ)]
6 + 6 = 12

5. (a) Explain Clock Gating. [(CO5)(Analyze/IOCQ)]
(b) Explain Dynamic Voltage Scaling (DVS). [(CO5)(Understand/LOCQ)]
6 + 6 = 12

Group - D

6. (a) For 3 input NAND gate, mention leaking transistors (channel leakage) for all possible combination of inputs. [(CO6)(Evaluate/HOCQ)]
(b) Explain how both channel and gate leakage can be reduced in FINFET transistor without compromising delay performance with respect to traditional transistor? [(CO6)(Analyze/IOCQ)]
6 + 6 = 12

7. (a) Sketch the Y chart for simplified VLSI design flow in three domains. [(CO1)(Remember/LOCQ)]

(b) Explain difference between pre-layout and post layout timing verifications.
[(CO1)(Analyze/IOCQ)]

6 + 6 = 12

Group - E

8. (a) Briefly explain interconnect capacitance components. [(CO3)(Analyze/IOCQ)]
(b) Why driver side of a wire needs to be low resistance and receiver side of the wire needs to be low capacitance, explain using Elmore Delay model.
[(CO3)(Analyze/IOCQ)]

6 + 6 = 12

9. (a) Write flow chart of VLSI Design and Verification Cycle.
[(CO1)(Remember/LOCQ)]
(b) What is parasitic Extraction and Back Annotation?
[(CO1)(Understand/LOCQ)]

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	37.5	37.5	25

Course Outcome (CO):

After the completion of the course students will be able to
1. Learn timing Verification flows
2. Learn Static Timing Analysis Method
3. Learn Interconnect Design
4. Learn Process Variation impact on design
5. Learn Dynamic Power Reduction Techniques
6. Learn Standby Power Reduction Techniques

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question