DIGITAL VLSI DESIGN
(ECEN 3201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

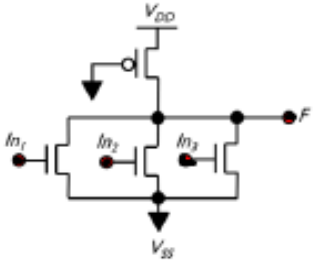
1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) According to Moore's Law, Number of Transistor per chip gets doubled in
(a) 12 months (b) 18 months
(c) 24 months (d) 30 months.

(ii) Latest integration technology is
(a) LSI (b) VLSI (c) ULSI (d) GSI.

(iii) Value of "Lambda" in 130nm process node is
(a) 130 nm (b) 45 nm (c) 65 nm (d) 90 nm.

(iv) What is the name of the given CMOS logic circuit?



(a) Pseudo-NMOS NOR gate (b) Pseudo-NMOS NAND gate
(c) PMOS only NOR gate (d) NMOS only NOR gate.

(v) Minimum number of transistors in CMOS logic Y = AB + CD is
(a) 10 (b) 12 (c) 14 (d) 8.

(vi) LUT belongs to below types of circuits
(a) Gate array (b) CPLD (c) PLA (d) FPGA.

(vii) What is the logical effort of "R" number of inputs in a NOR logic gate?
(a) 2R/3 (b) (R+1)/3 (c) (2R+1)/3 (d) none of these.

(viii) Most noise immune logic family is
(a) NMOS (b) Pseudo NMOS (c) Dynamic (d) CMOS.

(ix) IDDQ fault occurs when there is
(a) increased voltage (b) increased power supply
(c) increased discharge (d) increased quiescent current.

(x) CMOS domino logic is same as _____ with inverter at the output line.
(a) clocked CMOS logic (b) dynamic CMOS logic
(c) gate logic (d) switch logic

Group - B

2. (a) Design a CMOS gate for the logic function $f(x_1, x_2, x_3)= \Sigma m(2,4,6,7)$. Mention the widths of the NMOS and PMOS for the above design so that the current driving capability remains same as that of the basic CMOS inverter. [(CO1,CO3)(Evaluate/HOCQ)]

(b) Implement Full Adder circuit using LUT. [(CO2)(Analyze/IOCQ)]

(6 + 2) + 4 = 12

3. (a) Clearly explain the different regions of operation of both pMOS and nMOS transistors in CMOS inverter using VTC curve. Clarify what change in the VTC will be observed if widths of the transistors in the pull down network (PDN) of the inverter is increased. [(CO2)(Remember/LOCQ)]

(b) What do you mean by dynamic power dissipation in CMOS inverter circuit? Explain mathematically. [(CO3)(Understand/LOCQ)]

(6 + 3) + 3 = 12

Group - C

4. (a) Draw circuit diagram of a D-Latch using CMOS Transmission Gate (TG). [(CO3)(Analyze/IOCQ)]

(b) Draw circuit diagram of a positive edge triggered D-flip flop using D-latch. [(CO3)(Analyze/IOCQ)]

(c) Explain Euler Path solution of a CMOS gate which represents function f = (A+BC)! (! Means Bar) and draw Stick Diagram of the same CMOS gate based on Euler path solution. [(CO4)(Evaluate/HOCQ)]

4 + 4 + 4 = 12

5. (a) Draw and explain 6-Transistor SRAM cell read “0” operation. [(CO3)(Understand/LOCQ)]

(b) Draw and explain Sense amplifier operation for SRAM memory. [(CO3)(Understand/LOCQ)]

(c) Draw and explain 1-transistor DRAM cell write “1” operation. [(CO3)(Understand/LOCQ)]

4 + 4 + 4 = 12

Group - D

6. (a) Write a Verilog code to simulate a positive edge triggered D-flip flop. [(CO4)(Create/HOCQ)]

   (b) Draw the block diagram and write a structural module code for a 4:1 multiplexer. [(CO2)(Analyze/IOCQ)]

   (c) Sketch a schematic circuit described by the following code. Simplify to a minimum number of gates.

```
module exercise (input  logic a, b, c,
                 output logic y, z);
assign y= a & b & c| a & b & ~c| a & ~b & c;
assign z=a & b | ~a & ~b;
endmodule.
```

[(CO1)(Create/HOCQ)]

3 + (2 + 4) + 3 = 12

7. (a) Discuss the limitations of RTL synthesis. [(CO5)(Remember/LOCQ)]

   (b) Write an HDL module for a 4:1 multiplexer. [(CO5)(Create/HOCQ)]

   (c) State with example the types of circuit modelling using HDL. What do you mean by bit swizzling? [(CO5)(Analyze/IOCQ)]

2 + 4 + (4 + 2) = 12

Group - E

8. (a) What is input test pattern to detect stuck-at-1 fault at the output of a 2 input NAND gate ? [(CO6)(Analyze/IOCQ)]

   (b) Explain D-algorithm using an example. [(CO6)(Analyze/IOCQ)]

   (c) Draw circuit diagram of scan flip flop and explain how it works. [(CO6)(Analyse/IOCQ)]

4 + 4 + 4 = 12

9. (a) Explain transistor stuck short problem using an example. [(CO6)(Analyze/IOCQ)]

   (b) Explain electromigration and self heating in interconnect. [(CO6)(Analyze/IOCQ)]

   (c) Explain HCI (Hot Career Injection) in NMOS devices. [(CO6)(Analyze/IOCQ)]

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	27.08	50	22.92

Course Outcome (CO):

After the completion of the course students will be able to

1. Students will be able to relate to different MOS structures and functions in order to apply the knowledge in building CMOS circuits
2. Students will learn VLSI Design Cycle, Style and Methodology.
3. Students will be able to determine logic and performance of CMOS combinational and Sequential Circuit including Memory Array Design.
4. Students will be able to construct Physical Layout Design and Stick Diagram of Digital Gates.
5. Students will be able to make use of various synthesis flow and HDL modeling in ASIC Semi Custom Design.
6. Students will be able to interpret Si Testing and Debug related algorithms and Fault Modeling.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question